

博士論文

Silicon Functional Nanoscale Structures and Bio/Ion-Sensor 〔 シリコンナノ機能構造及び バイオ/イオンセンサーの研究 〕

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目次

1. 主論文

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2. 公表論文

- (1) “Fabrication of Si Nanowire Field-Effect Transistor for Highly Sensitive, Label-Free Biosensing”
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 - (3) “Biomolecule detection based on Si single-electron transistors for highly sensitive integrated sensors on a single chip”
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 - (4) “Biomolecule detection based on Si single-electron transistors for practical use”
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Applied Physics Letters, **103**, 043702-1 - 043702-4 (2013).
 - (5) “Characteristics of metal–oxide–semiconductor field-effect transistors with a functional gate using trap charging for ultralow power operation”
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主論文

Table of Contents

Chapter 1 Introduction

1. Introduction	1
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Chapter 2 Basic Knowledge and Background

2.1. Basic Knowledge	9
2.1.1. Ion Sensitive Field Effect Transistor	9
2.1.2. Biosensor	11
2.1.3. Debye length	12
2.1.4. Percolation Model	13
2.2. Background	15
2.2.1. Silicon Nanowire and Thin Gate Insulator for High Sensitivity	15
2.2.2. Method for the Increase in Detection Sensitivity of Biosensor	16
2.2.3. Detection of Streptavidin Utilizing Biotin-Streptavidin Specific Binding	17
2.2.4. Detection of Prostate-Specific Antigen Utilizing Biosensor	19
2.2.5. Ultimate Detection Sensitivity	21

Chapter 3 Fabrication Process and Measurement Setup

3.1. Fabrication Process Flows	25
3.2. Common Fabrication Process	27
3.2.1. Cleaning of the SOI wafer	27
3.2.2. Thinning the Top Silicon layer by Oxidation	28
3.2.3. Forming of Alignment Marks	30

3.2.4. Ion Implantation for Forming Source/Drain Regions	32
3.2.5. Forming of Contact Hole and Al Electrodes	33
3.3. Measurement Setup	33

Chapter 4 Silicon Functional Nanoscale Structures

4.1. Thin gate insulator	35
4.2. Silicon nanowire	36
4.3. Multiple Coulomb Islands with nanowire barriers	37
4.4. New Functional Gate MOSFET for Low Power	39
4.4.1. Principle of New Functional Gate MOSFET for Low Power	39
4.4.2. Device Structure and Fabrication Process	41
4.4.3. Result	42
4.4.4. Discussion	50
4.4.5. Summary	56

Chapter 5 pH Sensor and Biosensor Using Silicon Nanowire FET with Thin Gate Insulator

5.1. Advantage of pH Sensor and Biosensor Using Silicon Nanowire FET with Thin Gate Insulator	59
5.2. Device Structure and Fabrication Process	59
5.3. Schematic Diagram of Measurement System	61
5.4. pH measurement	61
5.5. Biomolecule Detection	64
5.6. Summary	67

Chapter 6 pH sensor and Biosensor Using Single Electron Transistor

6.1. Advantage of Biosensor and Ion (pH) Sensor Using Single Electron Transistor	68
6.2. Device Structure and Fabrication Process	73
6.3. Ion Sensor Using Single Electron Transistor.....	75
6.3.1. Measurement System for Ion Sensor	75
6.3.2. Electric characteristics of Single Electron Transistor	76
6.3.3. pH Measurement	76
6.4. Biosensor Using Single Electron Transistor	79
6.4.1. Measurement System	79
6.4.2. Si ₃ N ₄ Gate Insulator Surface Chemical Modification	80
6.4.3. Streptavidin Detection	83
6.4.4. Prostate Specific Antigen (PSA) Detection	85
6.5. Summary	86

Chapter 7 Conclusion

7.1 Conclusion.....	89
7.2 Academic Impact	91
7.3 Industrial Impact.....	91

Acknowledgements	92
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Appendix A. Process sheet of the functional gate MOSFET	93
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Appendix B. Process sheet of the SiNW-FET	97
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Appendix C. Process sheet of the Si-SET	100
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Chapter 1 Introduction

1. Introduction

Many types of devices and materials which lead to practically tools in our life have been developed with the functional nanoscale structure by the development of nanotechnology. In conventional flash memory, maximum amount of storage capacity on single chips increase by shrinking the size [8]. Semiconductor lasers with quantum dots in their active region are expected to exhibit ultralow threshold currents and temperature insensitive operation [9]. Also, the single-electron devices utilizing the Coulomb blockade effect are expected for basic elements of future low power, high density integrated circuits [10-16]. In this way, the device utilizing the functional nanoscale structure has a potential to make our life comfortable.

The purpose of the study is to fabricate and investigate silicon nanoscale structures having potential to be utilized for realizing various functional devices and show the advantages. The purpose includes the realization of high sensitive ion sensors and biosensors using the nanoscale structures. In this study, various type of silicon nanoscale structures have been fabricated and applied to the functional devices such as a functional gate metal-oxide-semiconductor field effect device (MOSFET), a silicon nanowire FET (SiNW-FET) with a thin gate insulator, and a silicon single-electron transistor (Si-SET). Here, one-dimensional nanoscale structure as to the tunnel gate oxide thickness and two-dimensional nanoscale structures as to the charge trap layer area were used in the functional gate MOSFET. On the other hand, the SiNW-FET with a thin gate oxide structure used two types of nanoscale structure. One type is a two-dimensional nanoscale structure as to the width/thickness of the nanowire and the other is a one-dimensional nanoscale structure as to the gate insulator thickness. Also, the Si-SET has the three-dimensional nanoscale structure as to the Coulomb islands and two dimensional nanoscale structures as to the nanowire barrier regions. These

SiNW-FETs and the Si-SETs were used to the ion and biomolecule sensors for highly sensitive detection.

The background as to the functional gate MOSFET is described [1, 2]. The extensive effort has been devoted to scaling metal–oxide–semiconductor field-effect transistors (MOSFETs) for low-power-consumption large-scale integrated circuits (LSIs) [17]. The use of high-k gate dielectrics has also been intensively studied as a means of power reduction [18, 19]. However, the fundamental difficulty in decreasing the threshold voltage (V_{th}) and/or S-factors (S denotes subthreshold swing) when scaling MOSFETs limits further reduction of the power supply voltage. Since power (P) is proportional to VDD (VDD is the power supply voltage) [18], lowering V_{th} by 0.1 V while keeping the gate overdrive voltage the same corresponds to a 20 % reduction in power consumption in advanced complementary metal–oxide–semiconductor (CMOS) LSIs. However, lowering V_{th} generally increases the off-current. To avoid this increase, either the S-factor has to be reduced or V_{th} has to be adjusted to a high value in the off-current state and a low value in the on-current state (meaning self-adjustment of V_{th}). To date, tunnel field-effect transistors (FETs) [20], ferroelectric-gate FETs [21, 22], and suspended-gate MOSFETs [23, 24] have attracted significant interest as ways to achieve S-factors lower than 60 mV/dec. However, there are still issues with these potential devices in terms of the process cost and compatibility with existing CMOS fabrication technology. In this study, I proposed a MOSFET with a functional gate that enables self-adjustment of V_{th} for low power operation and carried out a systematic study on the fundamental device characteristics necessary for ultralow power logic operation, while putting emphasis of the device reliability by assessing the endurance characteristics of the tunnel and lower gate oxides, their dependence on the scaling of the channel size, and a discussion of the breakdown mechanism.

In this study, the SiNW-FET and Si-SET have been fabricated using the fabricated silicon nanoscale structures for sensors enabling to detect ion and biomolecule with high sensitivity [3-7].

The detection and quantification of chemical and biological species are central to many areas of healthcare and life sciences, ranging from the diagnosis of disease to the discovery of new drug molecules. FETs are sophisticated devices used for the detection of charged molecules [25-37]. Ion-sensitive FET (ISFET) change their electrical characteristics in response to the concentration and type of ions present in aqueous solutions on the gate insulator surface [25, 30, 34-37]. Furthermore, biosensors and biochips based on FETs have recently been developed for the detection of DNA, proteins, and viruses [26-20, 31-33]. These methods are used to measure changes in charge accompanied by specific molecular recognition events on the gate insulator surface of FETs. One way to realize high sensitivity in detecting target ions or biomolecules is the use of SiNW-FET sensors [26, 27, 29, 32, 33]. SiNW-FETs are substantially more sensitive than conventional FETs because electrons or holes in a very narrow channel are more efficiently affected by charges on the gate insulator than those in a wide channel. Therefore, SiNW-FETs are suitable candidates for use in highly sensitive, label-free biosensing. However, FET sensors with even higher sensitivity in detecting targets are preferable, especially in dilute solutions of targets, where large noise exists in the drain current (I_d)-gate voltage (V_g) characteristics. Therefore, SiNW-FET sensors with an extremely thin gate insulator were proposed for highly sensitive ion and/or biomolecule detection in this study [3, 7]. Generally, SiO₂, Si₃N₄, Al₂O₃ and Ta₂O₅ are used for gate insulator of ion sensor and biosensor [34-37]. However, the use of a single layer of SiO₂ is difficult for the gate insulator because of the formation of leakage path through solution. Therefore, stack gate insulators of Si₃N₄/SiO₂ were fabricated in this study since the Si₃N₄/SiO₂ gate insulator reduce leakage currents compared with that of SiO₂, and the stack gate can be easily fabricated with LSI technology. The thickness of the fabricated Si₃N₄/SiO₂ gate insulator for ion sensor and biosensor was extremely thinner (42 nm Si₃N₄/10 nm SiO₂ for ion sensor and 19 nm Si₃N₄/8 nm SiO₂ for biosensor) compared with other researches (approximately Si₃N₄ 100nm/ 100nm SiO₂) [31, 37].

Furthermore, ion and biomolecule sensors utilizing a Si-SET have been proposed in this study [4-6]. High resolving power of ion and/or biomolecule concentration can be expected using Coulomb oscillation. Since room-temperature operation is necessary for ion and/or biomolecule detection, a multiple-island system is effective for Si-SETs. Moreover, a silicon structure is important since we can use existing large scale integration (LSI) technology in the fabrication and the fabricated Si-SET sensors can be integrated on a single chip for simultaneous detection and quantification of various ions and/or biomolecules. Therefore, in this study, Si-SET sensors with multiple islands were fabricated for highly sensitive ion/biomolecule detection and demonstrated their fundamental electrical characteristics.

In the devices investigated in this study, scaling down the device size improves their device performances (sensitivity and power consumption), which corresponds to the device scaling law. All dimensions of nanostructure (from one dimension to three-dimension) were investigated: The fabricated devices cover all dimensions of nanostructure.

The contents of this thesis are as follows. In Chapter 1, the introduction of this study is described. In Chapter 2, the basic knowledge and background for biosensor and ion sensor are described. In Chapter 3, common device processes are described. In Chapter 4, the silicon nanoscale functional structure including functional gate MOSFET for low power are described. In Chapter 5, pH and silicon-tag measurements using SiNW-FETs with a thin gate insulator are demonstrated. In Chapter 6, the detections of streptavidin and Prostate Specific Antigen (PSA) using Si-SETs are demonstrated. In Chapter 7, this study is concluded.

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Chapter 2 Basic Knowledge and Background

2.1 Basic Knowledge

Here, the basic knowledge necessary for this study is described.

2.1.1 Ion Sensitive Field Effect Transistor

Ion sensitive field effect transistor (ISFET) was developed by Bergveld [1, 2]. Figure 2.1 shows the conventional schematic diagram of ion sensitive field effect transistor (ISFET) by utilizing SOI wafer. The structure of ISFET is similar to that of the conventional field effect transistor (FET) except that the metal gate electrode is removed in order to expose the underlying insulator layer to solution. The gate insulator plays a role of ion response film and its surface potential can be detected by the FET. Also, the reference electrode is used to control the gate voltage of the ISFET through a solution. ISFET have the advantage of rapid response, small size, low cost and low output impedance, and are extremely attractive for biomolecule detection.

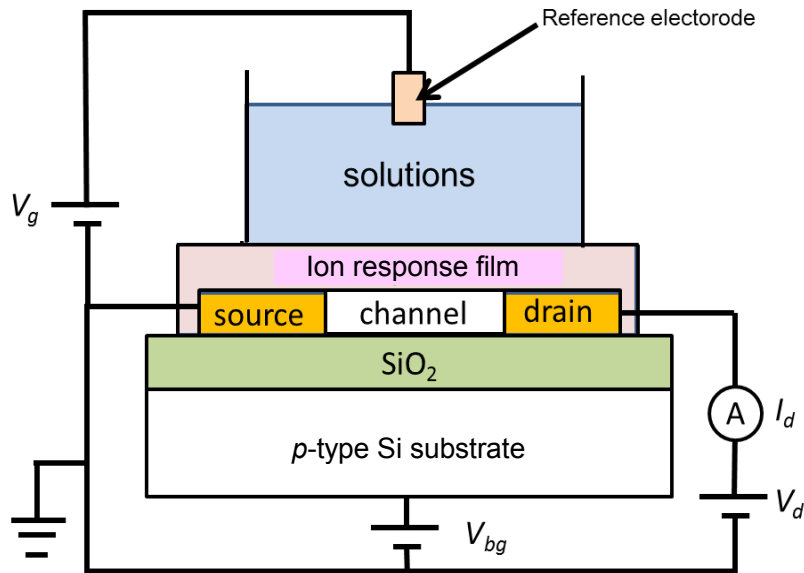


Fig. 2.1. Concept diagram of ISFET

The chemical response of ISFET depends on its ion response films. When the material such as SiO₂, Si₃N₄, Al₂O₃ and Ta₂O₅ can be selected as an ion response film of ISFET, ISFET is available as a pH sensor responding to a hydrogen ion [3-8]. A nearly ideal pH response, excellent stability and selectivity to other cations are obtained using Al₂O₃ or Ta₂O₅ [3, 6]. On the contrary, SiO₂ shows a poor response [3]. Moreover, it was proved that the oxygen content in Si₃N₄ surface degrades its properties as a pH sensor [3]. The following is interface potential mechanism in a solution [4]. Chemical structure of the surface of Si₃N₄ film is not the same to that of SiO₂ film. However, it is considered that SiOH sites are formed when the Si₃N₄ film is immersed in a solution [8]. The SiOH sites response to the change in H⁺ concentration (pH) as shown in Fig. 2.2.

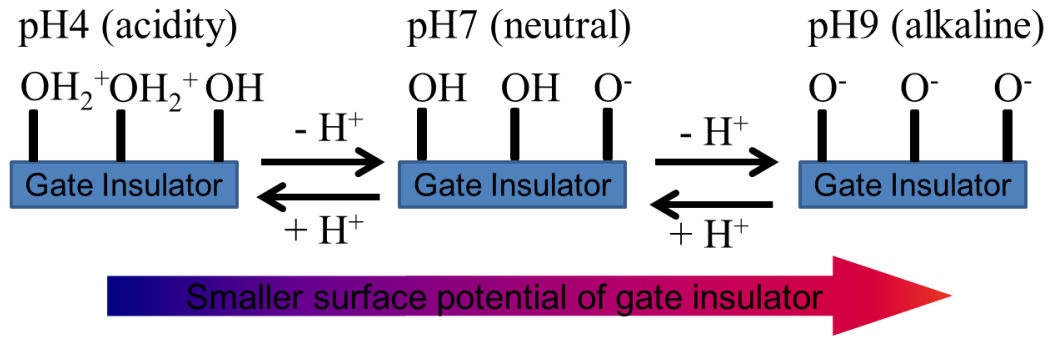


Fig. 2.2. The principle of ISFET

Therefore, ISFET with gate insulator responding hydrogen plays a role of pH sensor since surface potential of gate insulator depends on pH of the solution, and the surface potential (E) follows the Nernst equation [3].

$$E \equiv E^o + \frac{2.303RT}{zF} \log(a_i + K_{ij}a_j) \quad (1)$$

Here, E^o is standard potential of the reference electrode, R is gas constant, T is absolute temperature

of system in Kelvin, z is the charge of the primary ion, F is the Faraday's constant, a_i is activity of primary ion, a_j is the activity of interfering ion and K_{ij} is the selectivity coefficient of the primary ion over the interfering ion. From Eq. (1), the variation of interface potential between gate insulator and solution is 58 mV/pH at 20 °C [3]. However, the measured values were smaller than this ideal variation due to the insulator quality. In the previous reports [3, 9], the shift value of E with pH of the SiO₂-gate ISFETs is relatively small (20 to 36 mV/pH). The Si₃N₄-gate ISFET has a better shift value of E than the SiO₂-gate ISFET (46 to 56 mV/pH). This variation in sensitivity is considered to be due to varying oxygen content in the Si₃N₄ layer. On the other hand, the Al₂O₃-gate oxide ISFET has shown almost ideal shift value of E (52 to 58 mV/pH).

2.1.2 Biosensor

The idea of gating the channel of a FET using the electrostatic interactions between charged molecules adsorbed on the surface of the channel are introduced to biosensors as well [10-13]. The principle of biosensor is based on the detection of charge change on the gate surface, which is induced by specific binding between receptor and target biomolecule. The schematic diagram of biosensor using SOI wafer is shown in Fig. 2.3. Receptors are immobilized on the surface of the gate insulator as shown in Fig. 2.3(a). The surface of gate insulator is immersed in a solution for measurement. The potential of measurement solution is controlled and fixed by the gate voltage (V_g) through the reference electrode. When the target biomolecules are contained in the solution, the specific binding occurs between the receptors and targets as shown in Fig. 2.3(b). Since the target biomolecule are charged in an aqueous solution, the event of specific binding can be detected by measuring a shift of the threshold voltage (V_{th}) or drain current (I_d). For example, when the n-channel FET is used for biosensor, the target with positive charges decreases the V_{th} and I_d increases.

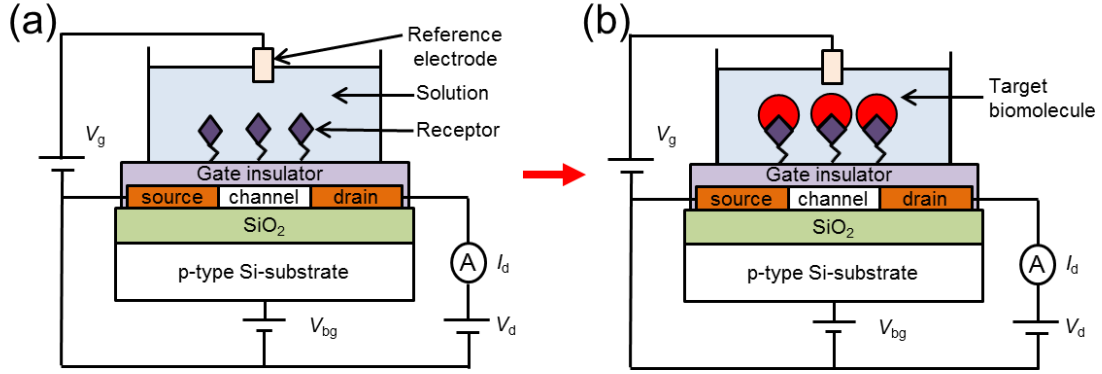


Fig. 2.3. The schematic diagram of biosensor using SOI wafer is shown in Fig. 2.3. (a) Receptors are immobilized on the gate surface. (b) Specific binding of receptors and target biomolecule.

2.1.3 Debye length

When biosensor utilizing FET is immersed in the buffer solution, an electric double layer is formed on the gate insulator surface with a thickness within the range of Debye length [14]. For aqueous solutions, this Debye length (λ_D) is given by

$$\lambda_D = \sqrt{\frac{\epsilon_w \epsilon_0 k T}{2 N_A e^2 \left(\frac{1}{2} \sum_i^n C_i z_i^2 \right)}} = \sqrt{\frac{\epsilon_w \epsilon_0 k T}{2 \times 10^3 N_A e^2 I}} \quad (2)$$

where ϵ_w is the permittivity of water at 25 °C, ϵ_0 is the vacuum permittivity, k is the Boltzmann constant, T is the absolute temperature in Kelvin, N_A is Avogadro constant, e is the elementary charge, C_i is the ion concentration in mol/m³, z_i is the ion charge, and I is the ionic strength of the buffer solution. In this Debye length, the electrical potential decreases as the position leaves away from the interface between gate insulator and buffer solution. In addition, the ISFET/biosensor is sensitive only to the charge within the Debye length because the targets charges are prevented by the charges of ions if the target charges are outside of Debye length. Therefore, the Debye length is one of the most important factors determining the detection limits of FET for biosensing in buffer

solution containing ions. The method for increasing Debye length is to decrease the concentration of ion in buffer solutions. However, reducing the ion concentration of buffer solutions has other a problem because it causes the collapse of the internal ionic balance of many biomolecules, especially protein, and causes severe denaturation that further degrades the detection sensitivity and actually interferes with the measurement. Another way to solve Debye length problem is the fabrication of the short probe molecules, which brings the target charges to the inside of Debye length. However, this method needs to special chemical reagents, such as papain and pepsin, and extra process for obtaining the target molecules. Therefore, the optimization of the Debye length is very difficult problem but is important for practical use.

2.1.4 Percolation Model

The time-dependent dielectric breakdown (TDDB) of oxide film is an important reliability issue of MOS/MOSFET integrated circuit [15]. About the oxide thickness longer than 5 nm, the percolation model well explains the mechanism of TDDB [15]. Figure 2.4 shows schematic diagram of TDDB mechanism from the percolation model. Electrons are trapped at random positions in the oxide film by the application of high voltage, and the number of the generated electron traps increase with the increased application time of voltage. The generation of electron traps continues with a conductive path is created from one interface to the other. This defines the breakdown condition. Only one such conductive path is enough to cause the oxide to break down.

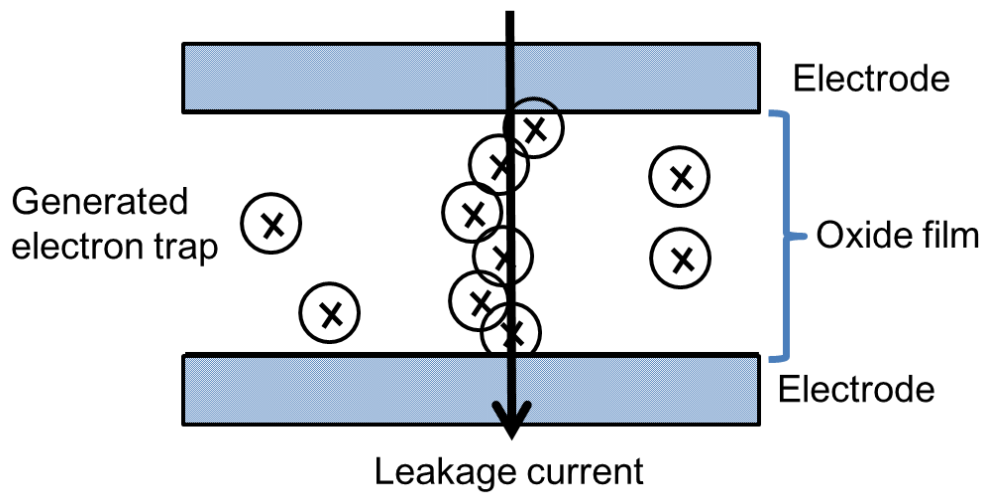


Fig. 2.4. Schematic diagram of oxide breakdown mechanism by percolation model

The probability of electron trapping in the oxide decreases for electron tunneling through the ultra thin oxide films as shown in Fig. 2.5.

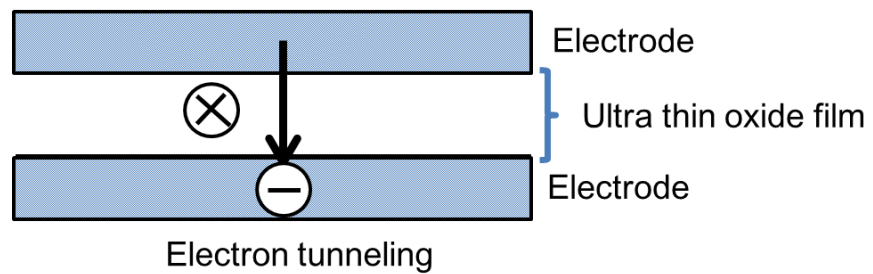


Fig. 2.5. Schematic diagram of thin oxide breakdown mechanism

2.2 Background

Here, the background of this study is described.

2.2.1 Silicon Nanowire and Thin Gate Insulator for High Sensitivity

The methods for the increase in sensitivity of ISFET are the usages of nanowire and thin gate insulator. Stern et al. measured the response of FETs with the different Si nanowire (SiNW) channel to five solutions with pH values varying from 6.0-8.0 as shown in Fig. 2.6(a) [13]. Since both an upper surface and two side surfaces are included in the surface area of SiNW fabricated by the top-down process, the surface areas of the SiNW increases with the increase in the width and thickness of the SiNW. One had the width of 1 μm and thickness of 80 nm, which resulted in large surface area of SiNW. The other had width of 100 nm and thickness of 25 nm, which resulted in small surface area of SiNW. Both SiNW-FETs responded appropriately to pH changes, with the small device exhibiting greater sensitivity: the pH 8.0/pH 6.0 current ratio was 43.8 versus 11.4 (for the smaller versus the larger SiNW-FETs, respectively). The impact of scaling on sensitivity is shown in Fig. 2.6(b) and the sensitivity (pH 8.0/pH 6.0 current ratio) increases with reduced channel surface area of SiNW. Therefore, it is important for the increase in the sensitivity of the sensor to reduce both of the SiNW width and thickness.

On the other hand, the thin gate insulators were effective for high sensitivity. In many of reports about ISFETs [3, 4, 16], thick gate insulators were necessary for preventing the leak path from forming in the insulators. For $\text{Si}_3\text{N}_4/\text{SiO}_2$ stack gate insulator, it was reported that the $\text{Si}_3\text{N}_4/\text{SiO}_2$ thickness was 70 nm/30 nm by Garde et al [16], 100 nm/600 nm by Esashi et al [4], and 100 nm/100 nm by Abe et al [3]. However, the increased thickness of gate insulator results in a decrease in transconductance. In the case, the change of drain current with a constant change of pH decreases, which leads to the smaller sensitivity. Therefore, it is important to reduce the thickness of the gate insulator keeping the leakage current extremely small.

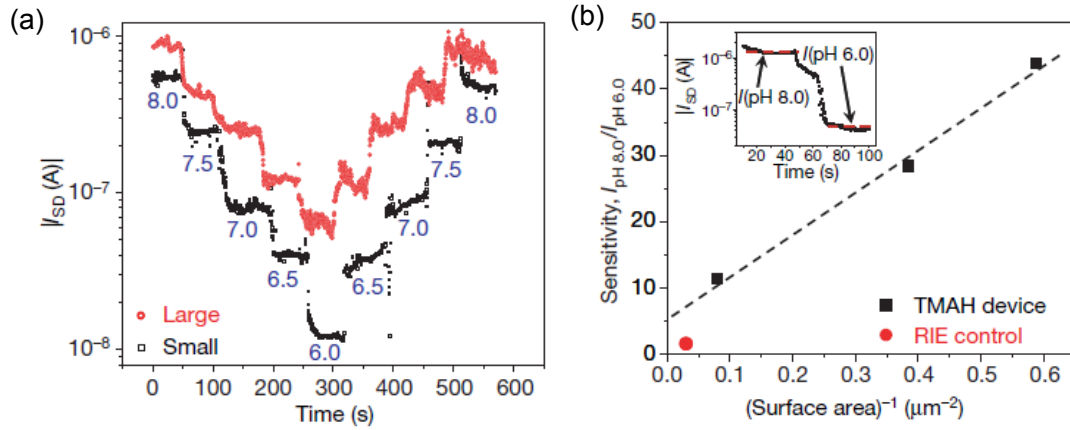


Fig. 2.6. (a) Response of two sensors to five solutions of different pH (indicated in blue). Large sensor: Si channel width (w) = 1 μm , Si channel thickness (t) = 80 nm. Small sensor: w = 100 nm, t = 25 nm. (b) Device sensitivity versus inverse device surface area. The inset shows the sensitivity definition [13].

2.2.2 Method for the Increase in Detection Sensitivity of Biosensor

The high sensitivity of biosensors is able to be realized by the scale down of the channel width [10-13]. The simulation results are shown in Fig. 2.7 by Nair et al [17], which shows that the conductivity (G_0) of the Si nanowire channel changes (ΔG) as target molecules are attached to the NW surface. To achieve Si nanowire structure necessary for high sensitivity, there are two types of the fabrication. One type is “bottom up” process [10, 12] such as the Si nanowire synthesized by the chemical vapor deposition using gold nanoclusters as catalysts, silane as reactant. However, the “bottom up” process causes several problems such as the difficulties in positioning of individual nanostructures, and the integration of sensor arrays. On the other hand, the “top-down” process for fabricating Si nanostructures provides a solution for manufacturing reliable biosensors since the “top down” process is compatible with the complementary metal oxide semiconductor technology. In the “top down” process, the Si channels are fabricated by utilizing lithography and dry/wet etching [11, 13].

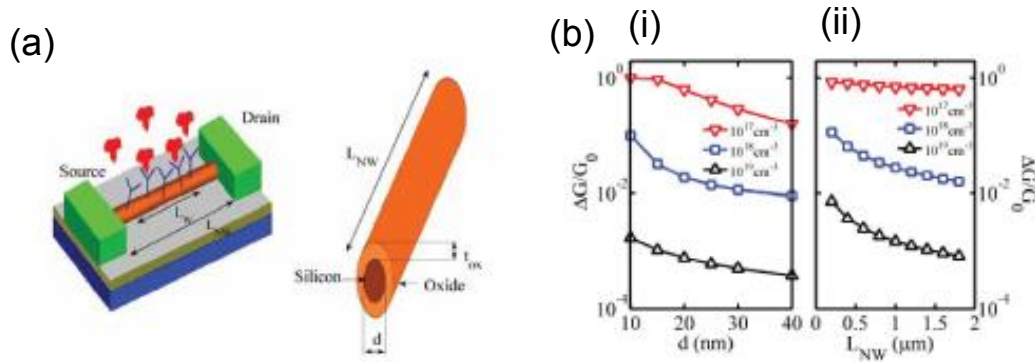


Fig. 2.7. (a) Schematic of a Si nanowire biosensor. The nanowire surface is functionalized with specific receptors to the targets. The conductance of nanowire changes as the target molecules are captured by the receptor. Here, L_{NW} is the length of the nanowire while L_W is the length over which surrounding fluid (air/water) interact with nanowire and t_{ox} represents the thickness of oxide layer on the nanowire. (b) Sensitivity of nanowire (*p*-type) for localized charge detection as a function of (i) diameter ($L_{NW} = 2 \mu m$ and $L_W = 1 \mu m$) and (ii) length ($d = 20$ nm, $L_W = L_{NW}/2$) for different doping densities. The charge is placed equidistant from the electrodes over a width of 8nm. (Charge ratio $CR = Qs(e.u)/d(nm) = 1/10$) [17].

2.2.3 Detection of Streptavidin Utilizing Biotin-Streptavidin Specific Binding

The biotin-streptavidin system is a widely used intermediate between the surface of gate insulators and the active biolayer. It is also employed as a model system to study biorecognition events between proteins and other biomolecules [18]. Biomolecules such as proteins and DNA can be easily biotinylated and bound to streptavidin coated surfaces. The biotin-streptavidin binding system is the most stable noncovalent biological binding couple known, with a binding affinity of $10^{15} M^{-1}$ for free complexes. This binding couple is highly stable under a wide range of conditions including extreme pH, salt concentration and temperature. For these advantages, the biotin-streptavidin specific binding is used for investigating feasibility of FET-type biosensor [12, 13].

In the recent researches of the biosensor utilizing SiNW-FET fabricated by top-down processes, Hsu et al. used SiNW-FET fabricated by silver assisted chemical etching [19]. 3-aminopropyltriethoxysilane (APTES) is used as interfacing molecules, and assembly of these

molecules is essential in surface modification technologies. Then they modified biotin on SiNW-FET to detect streptavidin. For SiNW-FET, variation in molecular charge is reflected in a change in the wire current. In the concentration dependent real-time measurement of biotin modified SiNW-FET, the detection limit of streptavidin was 10^{-8} M ($= 0.53$ $\mu\text{g/ml}$) as shown in Fig. 2.8.

Also, Stern et al. fabricated SiNW-FETs by a top-down process and using an anisotropic wet etching [13]. An exploration of the detection limit of these sensors is shown in Fig. 2.9, where streptavidin concentrations are decreased from 1 nM to 10 fM ($=0.53$ pg/ml). Close inspection of the post-transition current reveals that the response at the highest protein concentrations saturates (probably fully coating the sensor with bound protein during solution exchange), whereas the signal continues to increase for proteins in the solutions of lower concentration, probably owing to continued diffusion and binding to the devices after initial mixing.

On the other hand, in the bottom-up process, Cui et al. used the single-crystal SiNW fabricated by a nanocluster-mediated vapor-liquid-solid growth method [12]. They explored the sensitivity limits of the fabricated biotin-modified SiNW nanosensors and found that it was possible to detect streptavidin binding down to a concentration of at least 10 pM ($= 0.53$ ng/ml) [Fig. 2.10].

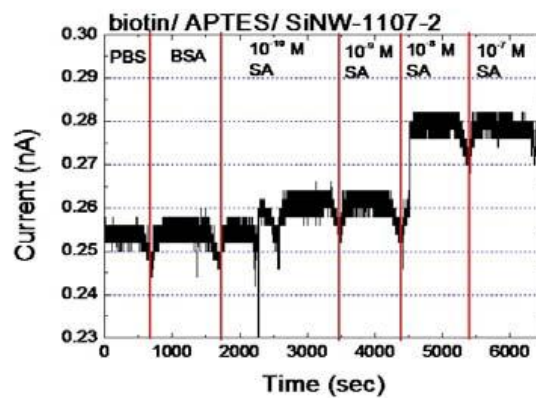


Fig. 2.8. Experimental result of streptavidin dose-response [19].

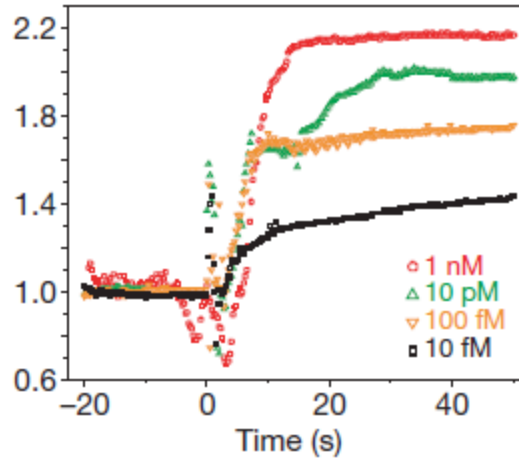


Fig. 2.9. Detection response with decreasing streptavidin concentration [13].

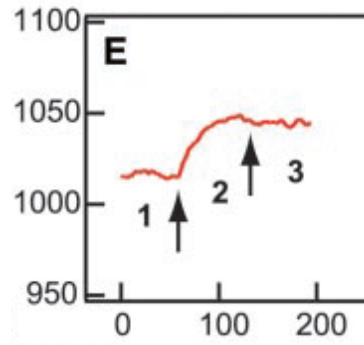


Fig. 2.10. Conductance versus time for a biotin-modified SiNW, where region 1 corresponds to buffer solution, region 2 corresponds to the addition of 25 pM streptavidin, and region 3 corresponds to pure buffer solution. Arrows mark the points when solutions were changed [12].

2.2.4 Detection of Prostate-Specific Antigen Utilizing Biosensor

Prostate-specific antigen (PSA) has truly revolutionized all aspects of the management of men with prostatic carcinoma [10, 11]. Its most important application is, of course, in the early detection or screening for this most common of all human malignancies. PSA has identified men at risk for cancer—and identified such malignancies at a curable stage.

For the fabricated nanowire by bottom up process, Zheng et al. described highly sensitive, label-free, multiplexed electrical detection of the PSA such as cancer markers using SiNW-FET in

which distinct nanowires and surface receptors are incorporated into arrays [10]. Cancer markers were routinely detected at femtomolar concentrations with high selectivity, and simultaneous incorporation of control nanowires enabled discrimination against false positives. Nanowire arrays allowed highly selective and sensitive multiplexed detection of PSA including detection to at least 0.9 pg/ml in undiluted serum samples as shown in Fig. 2.11.

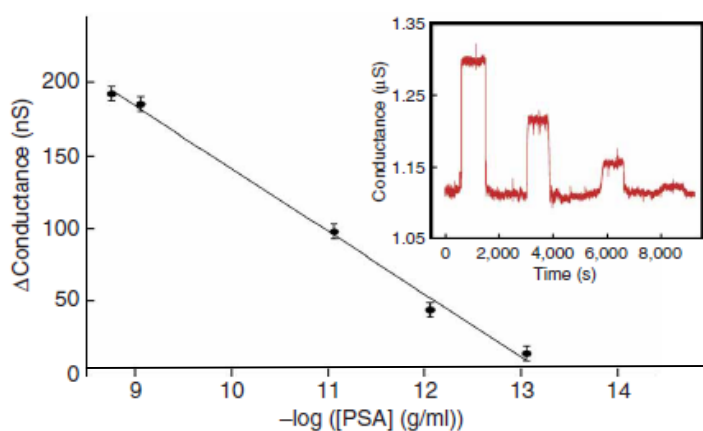


Fig. 2.11. Change in conductance versus concentration of PSA for a p-type SiNW modified with PSA-Ab1 receptor. Inset: Conductance-versus-time data recorded after alternate delivery of PSA and pure buffer solutions; the PSA concentrations were 0.9 ng/ml, 9 pg/ml, 0.9 pg/ml and 90 fg/ml, respectively. The buffer solutions used in all measurements were 1 mM phosphate (potassium salt) containing 2 mM KCl, pH = 7.4 [10].

On the other hand, Kim et al. reported that ultrasensitive, label-free, and real-time PSA sensor was developed using n-type SiNW-based structures configured as field-effect transistors using the conventional “top-down” semiconductor processes [11]. Specific binding of PSA with antibody of PSA (anti-PSA) immobilized on the Si surface through covalent linkage leads to a conductivity change in response to variations of electric field at the surface. The conductance changes depending on PSA concentrations and pH values in solution according to isoelectric point of PSA provide the evidence of the real-time detection of 1 fg/ml PSA as shown in Fig. 2.12.

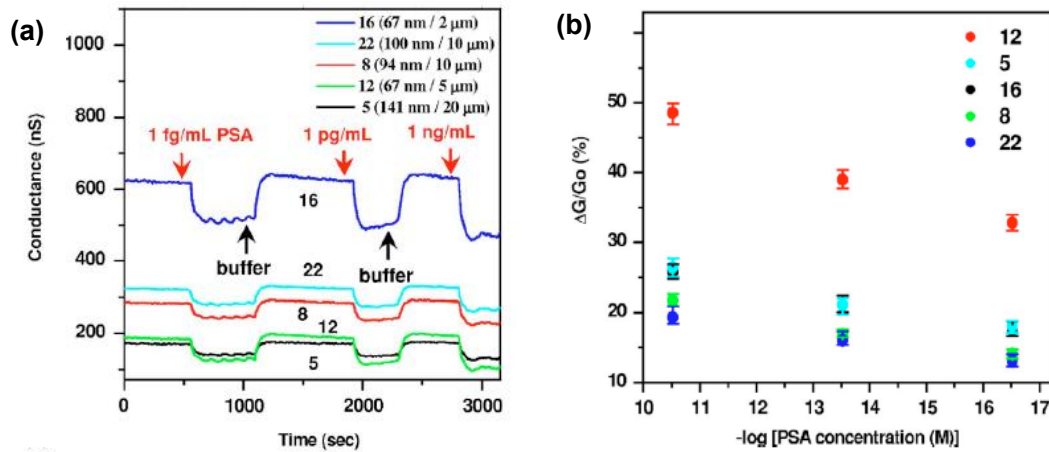


Fig. 2.12. Real-time electrical detection of PSA. (a) Conductance vs. time data recorded with five different *n*-type Si-FETs simultaneously after reversible injection of buffer and PSA with three different PSA concentrations, which are 1 fg/ml, 1 pg/ml, and 1 ng/ml. The dimensions of five Si nanochannels are indicated on the graph (channel number and width/length). (b) Sensitivity vs. logarithm of PSA concentration data [11].

2.2.5 Ultimate Detection Sensitivity

Ultimate detection sensitivity of FET-based biosensor is detection of single-level target. Patolsky et al. reported direct, real-time electrical detection of single virus particles with high selectivity by using nanowire field effect transistors [20]. Measurements made with nanowire arrays modified with antibodies for influenza A showed discrete conductance changes characteristic of binding and unbinding in the presence of influenza A but not paramyxovirus or adenovirus as shown in Fig. 2.13(a). Simultaneous electrical and optical measurements using fluorescently labeled influenza A were used to demonstrate conclusively that the conductance changes correspond to binding/unbinding of single viruses at the surface of nanowire devices as shown in Fig. 2.13(b). pH-dependent studies further show that the detection mechanism is caused by a field effect, and that the nanowire devices can be used to determine rapidly isoelectric points and variations in receptor-virus binding kinetics for different conditions as shown in Fig. 2.13(c). Lastly, studies of nanowire devices modified with antibodies specific for either influenza or adenovirus show that

multiple viruses can be selectively detected in parallel as show in Fig. 2.14. The possibility of large-scale integration of these nanowire devices suggests potential for simultaneous detection of a large number of distinct viral threats at the single virus level.

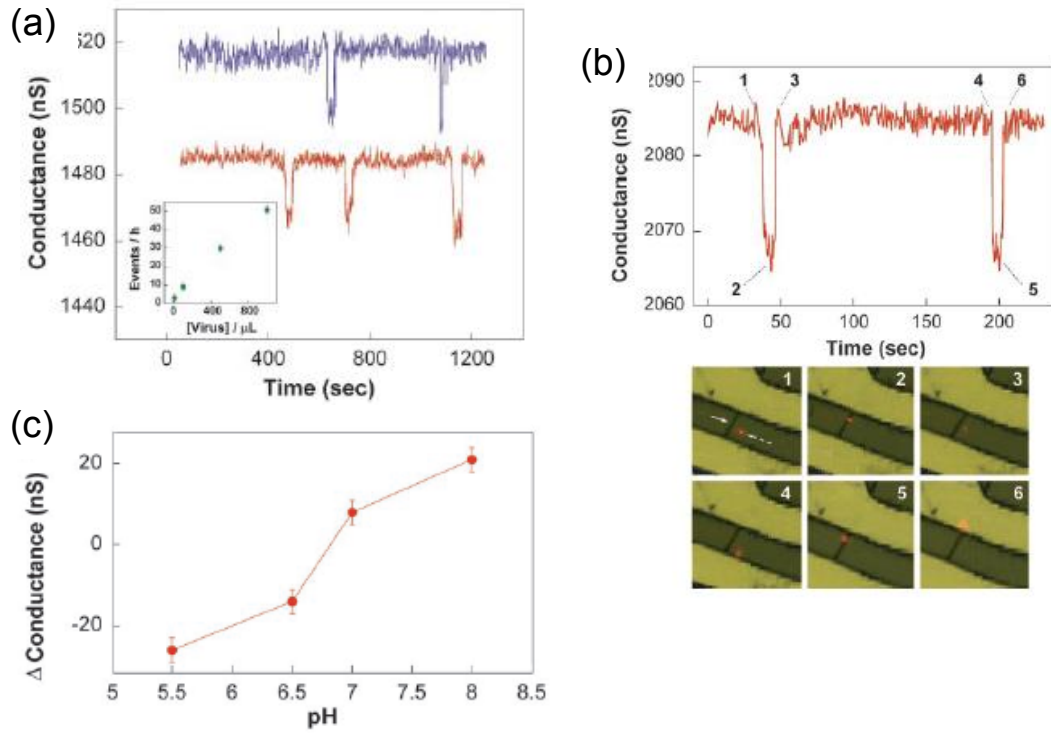


Fig. 2.13. Selective detection of single viruses. (a) Conductance vs. time data recorded simultaneously from two SiNWs, red and blue plots, within a single device array after introduction of an influenza A solution. (*Inset*) Frequency of single virus events as a function of virus solution concentration. (b) Conductance (*Upper*) and optical (*Lower*) data recorded simultaneously vs. time for a single SiNW device after introduction of influenza A solution. Combined bright-field and fluorescence images correspond to time points 1–6 indicated in the conductance data; virus appears as a red dot in the images. The solid white arrow in image 1 highlights the position of the nanowire device, and the dashed arrow indicates the position of a single virus. Images are $8 \times 8 \mu\text{m}$. (c) Conductance changes associated with single influenza A virus binding/unbinding as a function of solution pH. All measurements were performed with solutions containing 100 viral particles per μl [20].

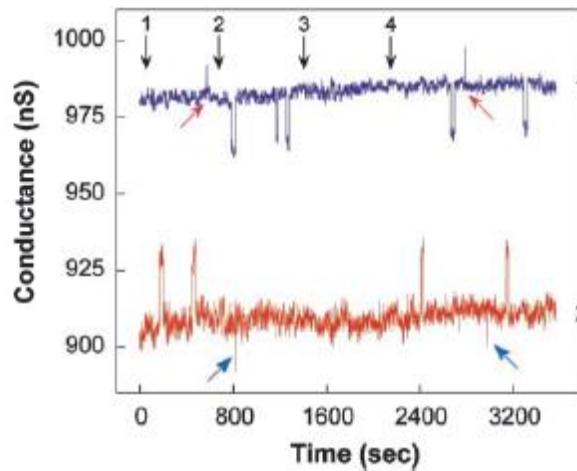


Fig. 2.14. Conductance vs. time data recorded simultaneously from two SiNWs; one nanowire (nanowire 1) was modified with anti-influenza type A antibody (blue data), and the other (nanowire 2) was modified with anti-adenovirus group III antibody (red data). Black arrows 1–4 correspond to the introduction of adenovirus, influenza A, pure buffer, and a 1:1 mixture of adenovirus and influenza A, where the virus concentrations were 50 viral particles per μl in phosphate buffer (10 μM , pH 6.0). Small red and blue arrows in B and C highlight conductance changes corresponding to diffusion of viral particles past the nanowire and not specific binding [20].

Reference

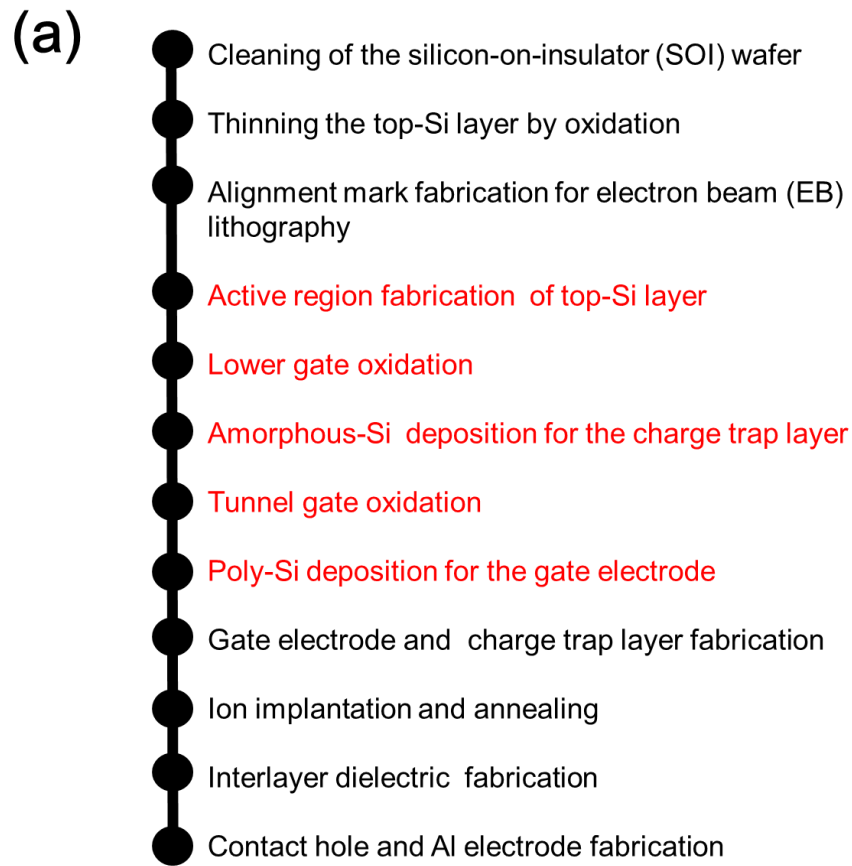
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Chapter 3 Fabrication Process and Measurement Setup

3.1 Fabrication Process Flows

Figure 3.1 shows the fabrication process flows about (a) the functional gate MOSFET, (b) silicon nanowire FET (SiNW-FET) and (c) silicon single-electron transistor Si-SET. A silicon-on-insulator (SOI) wafers were used for the device fabrication. The schematic diagram and the initial parameters of the SOI wafers are shown in Fig 3.2 and table 3.1, respectively.



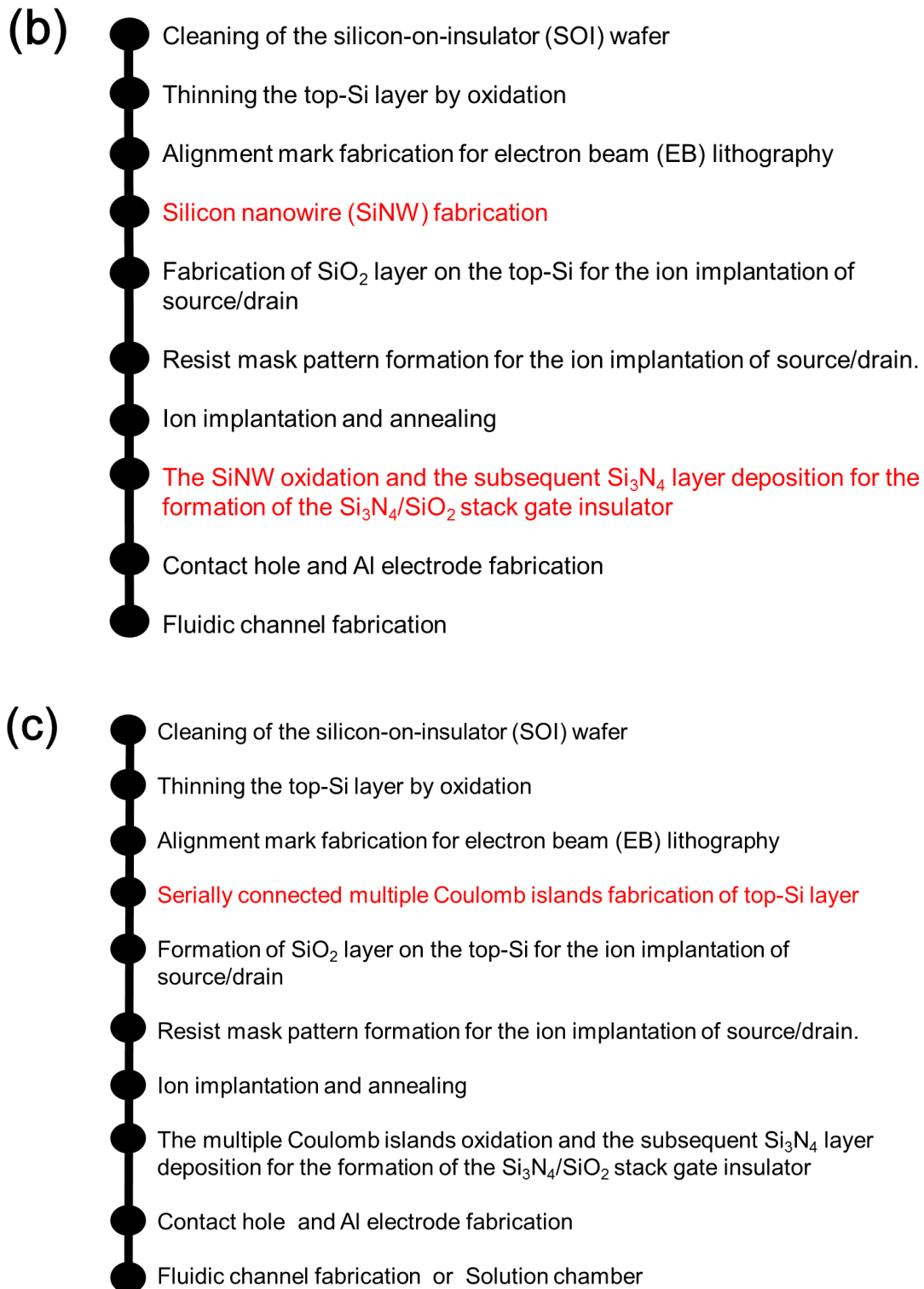


Fig. 3.1. Flows of fabrication process. (a) Functional gate MOSFET. (b) SiNW-FET. (c) Si-FET. Common processes and described in black and the key process for each device is described in red.



Fig 3.2. Schematic diagram of SOI wafer.

	Parameters	Functional gate MOSFET	SiNW-FET	Si-SET
Top Silicon layer	Thickness [nm]	71-78	65-71	157-160
	Doping type / species	p-type / Boron		
	Resistivity [$\Omega \cdot \text{cm}$]	14-22		
	Crystal orientation	<100>		
Buried oxide	Thickness [nm]	200	400	400
Silicon substrate	Thickness [nm]	0.25mm		
	Doping type / species	p-type / Boron		
	Resistivity [$\Omega \cdot \text{cm}$]	14-22		
	Crystal orientation	<100>		

Table 3.1. The initial parameters of SOI wafer for each device.

3.2 Common Fabrication Process

Here, the common fabrication processes are described. As to the individual process to exhibit the advantage of devices, the each chapter is described.

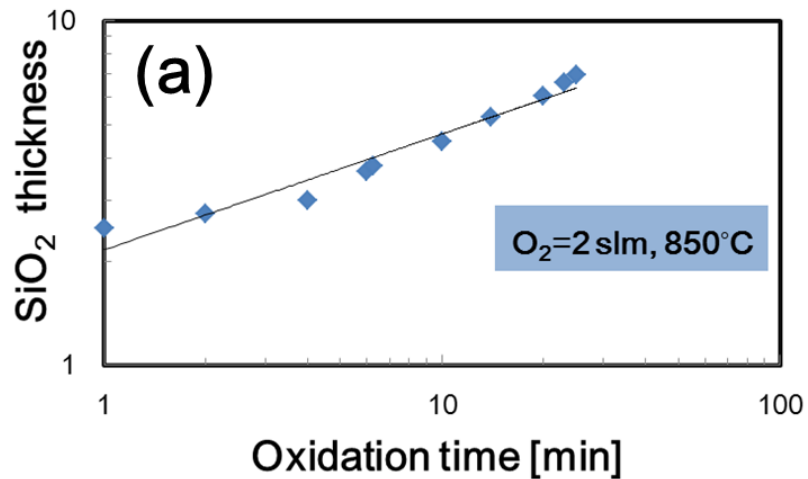
3.2.1 Cleaning of the SOI Wafer

The SOI wafer was cleaned by sulfuric acid hydrogen peroxide mixture (SPM) process to remove organic materials on the top-Si. The mixture ratio of the used SPM is H_2SO_4 (98wt.%) / H_2O_2 (30wt.%) is about 3:1. Since the SPM has strong oxygenation, organic materials are decomposed into CO_2 or H_2O , which results in the removal of organic contamination from the top-Si of SOI wafer. After the SPM cleaning for 10 min, the SOI wafer is rinsed by pure water and dried by a spin dryer. The subsequent SC-1 cleaning was carried out to remove particles such as metal particles. The prepared SC-1 cleaning solution is composed of NH_4OH (10wt.%) / H_2O_2 (30wt.%) / H_2O (100wt.%)

and the mixtures rate is 0.15:3:7. After SC-1 cleaning for the 10 min at 80 °C, the SOI wafer was rinsed by pure water. Here, it is necessary to be careful when utilizing SC-1 cleaning since the SC-1 cleaning includes wet etching effect. When the SC-1 cleaning process was finished, the approximately 3nm of the top-Si thickness was etched and the chemical SiO₂ layer was formed on the surface of top-Si. To remove the chemical SiO₂ layer, the SOI wafer was immersed in HF solution of 0.5% for 10min. The surface of top-Si showed the nature of water repellency by the removal of chemical SiO₂ layer.

3.2.2 Thinning the Top Silicon layer by Oxidation

The thickness of the top-Si layer of the SOI wafer was reduced to about 30nm by oxidation. Since about 44% of the formed SiO₂ layer thickness is that of the consumed top Si by oxidation, about 88 nm of the SiO₂ layer thickness was calculated to be necessary to obtain 30 nm thickness of the top-Si. By the preliminary oxidation utilizing bare Si wafers, the accurate oxidation rates were obtained: The obtained oxidation rates are shown in Fig 3.3. From the results, the oxidation conditions were determined as shown in Table 3.2, which results in the thickness of SiO₂/top-Si as shown in Fig 3.4.



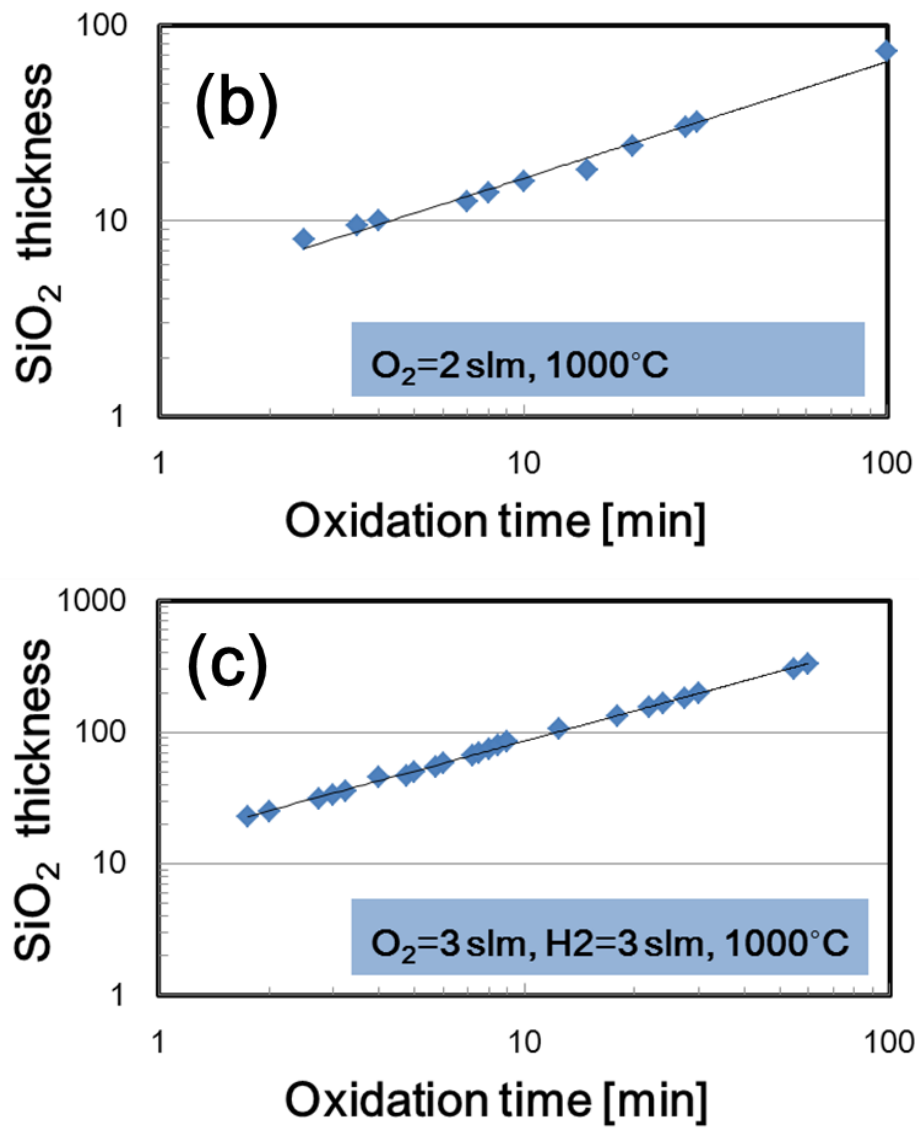


Fig. 3.3. Oxidation rate of Si. (a) O₂=2 slm at 850°C. (b) O₂=3 slm at 850°C. (c) O₂=3 slm, H₂=3 slm at 850°C.

	Oxidation condition	SiO ₂ / top-Si thickness
Functional gate MOSFET	O ₂ =2 slm/1000°C/3min30sec	9nm/70nm
SiNW-FET	O ₂ =2 slm/1000°C/100min	68nm/35nm
Si-SET	O ₂ =3 slm, H ₂ =3slm /1000°C/30min →HF wet etching for SiO ₂ →O ₂ =3 slm, H ₂ =3slm /1000°C/7min	65nm/37nm

Table 3.2. Oxidation condition.



Fig. 3.4. Schematic diagram after thinning the top-Si.

3.2.3 Forming of Alignment Marks

Electron beam (EB) lithography process was used for fabricating resist mask pattern. Therefore, it is necessary to form Alignment marks on the SOI wafer for the alignment of resist mask pattern of EB lithography. The resist mask pattern of the alignment marks were formed by EB lithography with a positive resist (ZEP520A). After EB lithography with dose of 90 $\mu\text{m}/\text{cm}^2$, the resist patterns were developed by immersing the SOI wafer in xylene for 10 min. Then, IPA rinse for 1 min and the subsequent pure water cleaning for 8 min were carried out, respectively. The microphotograph of the formed resist mask pattern of alignment marks are shown in Fig 3.5.

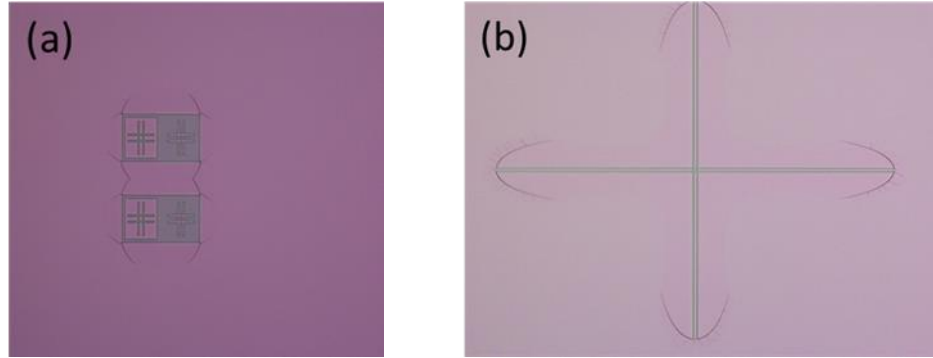


Fig. 3.5. Mask pattern of alignment mark.

Using the formed resist pattern as a mask, marks were etched on the SOI wafer by utilizing dry etchings. Dry etchers of reactive ion etching (RIE) and electron cyclotron resonance (ECR) were used. First, SiO_2 layer formed on the top Si was etched by using RIE for about 150 sec. The used gas was mixtures of CF_4 (20 sccm)/ H_2 (7 sccm). Next, the top-Si layer was etched for about 90 sec. Then, only CF_4 gas was used. After that, the SiO_2 layer (buried oxide layer in the SOI wafer) was etched for 14 min. The used gas was a mixture of CF_4/H_2 again. Finally, by utilizing ECR etcher, the Si substrate of SOI wafer is etched about 100 nm by using ECR etcher. The used gas is Cl_2 (40 sccm).

After the etching, the resist mask patterns were removed by ashing and SPM cleaning. The microphotograph of the formed alignment marks (wafer and chip marks) are shown in Fig 3.6.

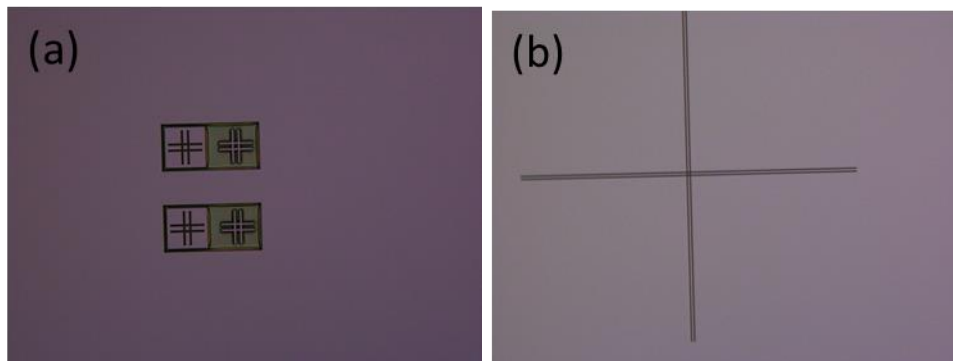


Fig. 3.6. Microphotograph of the fabricated alignment marks.

To remove the top SiO₂ layer, wet etching was performed by using buffed hydrofluoric acid (BHF). BHF is composed of buffering agent such as ammonium fluoride (NH₄F) and hydrofluoric acid (HF). The schematic diagram after top SiO₂ layer wet etching is shown in Fig. 3.7.



Fig. 3.7. Schematic diagram after the top-SiO₂ wet etching.

3.2.4 Ion Implantation for Forming Source/Drain Regions

To make source/drain regions for SiNW-FET and Si-SET except for the functional gate MOSFET, the active area except for source/drain region was necessary to be covered with a resist (SAL601-SR7) mask pattern. After EB lithography with dose of 30 $\mu\text{C}/\text{cm}^2$, the resist mask pattern was developed by using CD-26 developer. The formed resist mask pattern is shown in Fig 3.8.

After that, As⁺ of $4 \times 10^{15}/\text{cm}^2$ was implanted into the source/drain region of top-Si. Then, the resist mask pattern was removed by ashing and SPM cleaning.

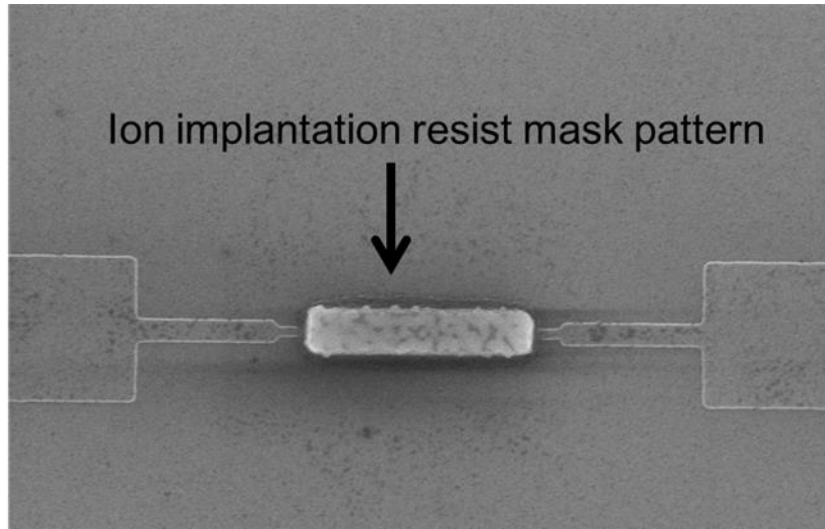


Fig. 3.8. Resist mask pattern for ion plantation.

3.2.5 Forming of Contact Hole and Al Electrodes

The contact holes and the Al electrodes were formed. The resist pattern for contact holes was formed on the Si_3N_4 layer by EB lithography. Then, Si_3N_4 layer was etched by chemical dry etching (CDE) and the subsequent SiO_2 layer etching was carried out by using BHF. After that, Al was deposited on the contact hole by using a vacuum deposition equipment. Then, Al electrode was fabricated by using EB and wet etching with H_3PO_4 .

3.3 Measurement Setup

Figure 3.9 shows the measurement set up for the measurement of electric characteristics by utilizing the semiconductor parameter analyzer B1500 (Agilent Technology) and the manual prober (Vector Semiconductor) for measurement of biosensors. For the measurement of the functional gate MOSFET, the 4156C and 41501B plus generator were used. When using B1500 or 4156C, each source/monitor unit (SMU) terminal was jointed to the manual prober to apply a gate voltage (V_g), a

drain voltage (V_d), a source voltage (V_s), and backgate voltage (V_{bg}). After that, the fabricated devices are set on a pedestal plate. More details of measurement conditions including wafer schematic diagrams are described in each chapter.

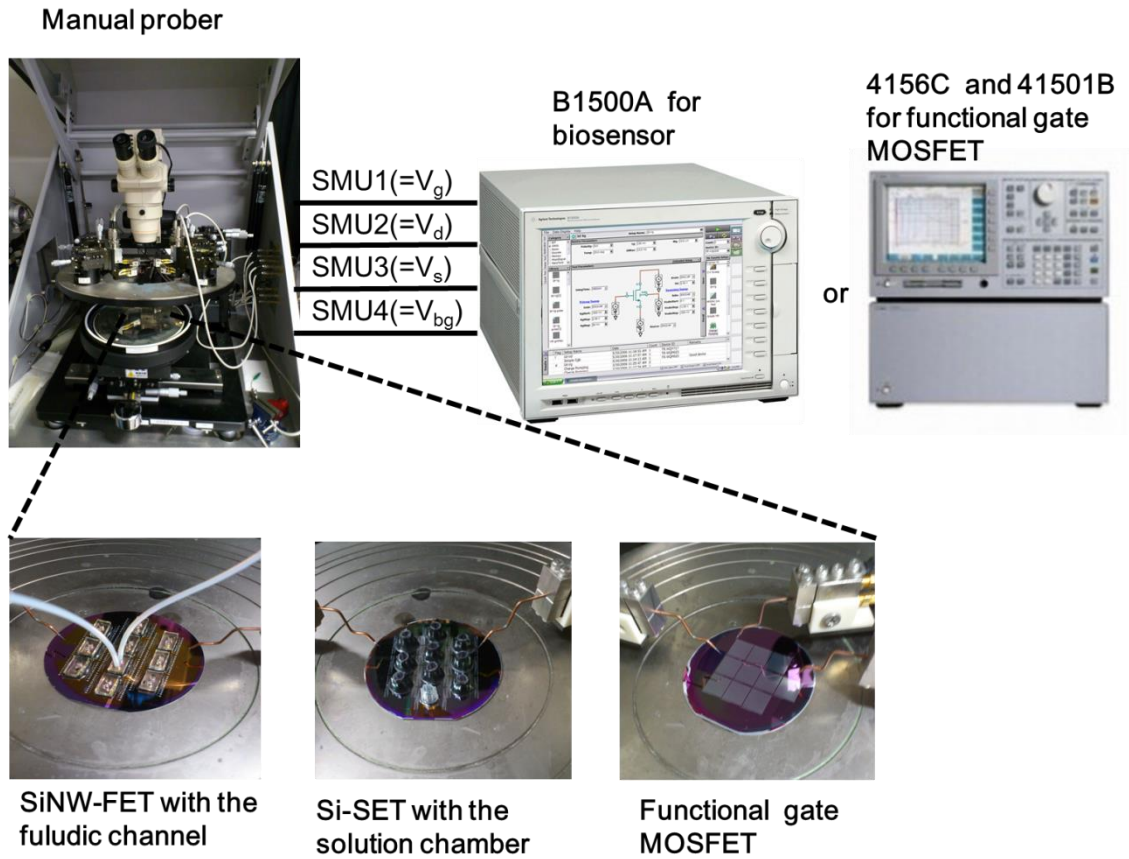


Fig. 3.9. Measurement set up.

Chapter 4 Silicon Nanoscale Functional Structures

4.1. Thin Gate Insulator

For biosensor and ion sensor, the thin gate insulator was fabricated on the silicon nanowire (SiNW). The fabrication procedure was as follows. Stacked gate insulators were fabricated by thermal oxidation and low-pressure chemical vapor deposition (LPCVD). In the SiNW field-effect-transistor (SiNW-FET) for pH measurement, the SiO₂ with a thickness of 10 nm was thermally grown at 850 °C in a dry atmosphere followed by the deposition of 42 nm-thick Si₃N₄ by LPCVD at 750 °C. A thin gate insulator (19 nm Si₃N₄/8 nm SiO₂) was also fabricated for monitoring the charge of Si-tag. For the stack gate insulator of the silicon single electron transistor (Si-SET), the thickness of SiO₂ was 9 nm and that of Si₃N₄ was 36 nm. For the stack gate insulator, the leakage currents between the reference electrode and the SiNW were not confirmed. For thin gate insulators than 19 nm (Si₃N₄)/8 nm (SiO₂), the drain current (I_d) - backgate voltage (V_{bg}) characteristics are shown in Fig. 4.1. When the gate insulator surface is immersed in the pure water, three measurements were carried out for each device. Since the I_d - V_{bg} curves did not coincide in the three measurements for the gate insulators of SiO₂ (2 nm) and Si₃N₄/SiO₂ (5 nm/2 nm), the leakage currents were caused between the reference electrode and the SiNW. When the stack gate insulator is applied to biosensors and ion sensors, the influence of target charges on the gate insulator increases with decreasing the thickness of the gate insulator. This leads to the high sensitive detection. Therefore, it is important to reduce the thickness of the gate insulator keeping the leakage current extremely small.

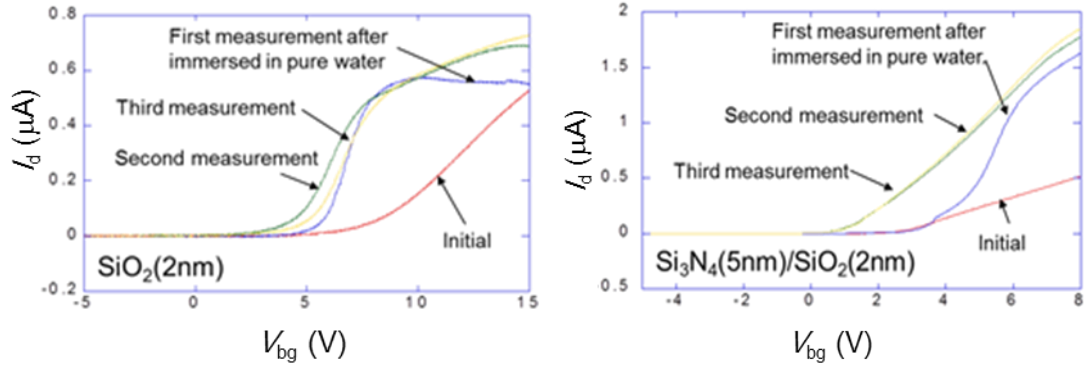


Fig. 4.1. The drain current (I_d) - backgate voltage (V_{bg}) characteristics with immersing in pure wafer. The gate insulators are (a) SiO_2 of 2 nm and (b) Si_3N_4/SiO_2 of 5 nm/2 nm.

4.2. Silicon Nanowire

The fabrication procedure of silicon nanowire (SiNW) for biosensor and ion sensor is described. The SiNW is fabricated from the top-silicon layer of silicon-on-insulator (SOI) wafer by using a top-down process. The thicknesses of the top-silicon layer (p-type, $10 \Omega \cdot cm$) and buried oxide layer of the SOI were 72 - 76 nm and 400 nm, respectively. To obtain a thin nanowire for high sensitivity, the thickness of the top-silicon layer of the SOI wafer was reduced to 30 nm by dry oxidation with flowing O_2 gas = 2 slm at 1000 °C. After that, the SiO_2 on the top silicon layer of the SOI was removed by BHF wet-etching. Next, a mask pattern of the SiNW was formed by electron beam (EB) lithography with a negative resist (SAL601-SR2). The top-silicon layer of the SOI was etched with the resist pattern using an electron cyclotron resonance etcher (ECR-etcher). Figure 4.2 shows a scanning electron micrograph of the fabricated structure after the etching [1]. Near the source and drain regions [Fig. 4.2(a)], the final width of the SiNW was approximately 80 nm. However, the width at the center of the SiNW is about 65 nm [Fig. 4.2(b)], which is smaller than that near the source and drain regions. This is considered to be due to the proximity effect of EB lithography. In nanowire FETs, high detection sensitivity is obtained due to the suppression of leakage current in I_d from the percolation paths through the channel even in the dilute range of target molecule concentration.

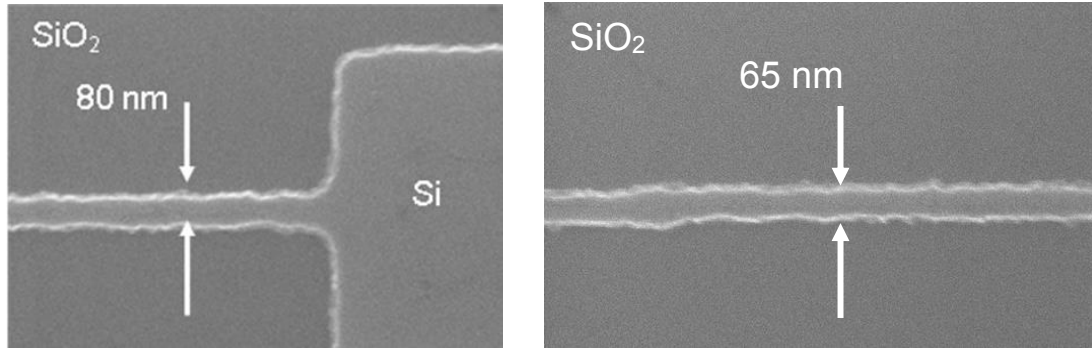


Fig. 4.2. Scanning electron micrograph of fabricated silicon nanowire [width: (a) 80 nm and (b) 65 nm [1].

4.3. Multiple Coulomb Islands with Nanowire Barriers

Multiple Coulomb islands with nanowire barriers were fabricated for high sensitivity in ion/biomolecule detection. Here, the fabrication process for the multiple Coulomb islands with nanowire barriers is described. A mask pattern has 11 islands and channel length of 3 μm as shown in Fig. 4.3. The widths of barrier vary and are 50 nm, 62.5 nm and 75 nm. The widths of Coulomb islands are larger than the width of the barrier by 12.5 nm or 25 nm.

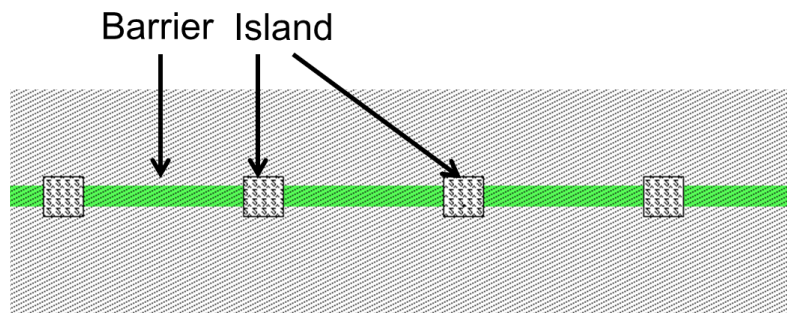


Fig. 4.3 A mask layer pattern of the multiple Coulomb Islands with nanowire barriers.

After thinning the thickness of top-silicon layer of a SOI wafer, the pattern of the multiple coulomb islands with nanowire barriers were formed by electron beam lithography with a negative resist (SAL601-SR2). The formed resist patterns are shown in Fig. 4.4. The serially connected multiple Coulomb islands were observed.

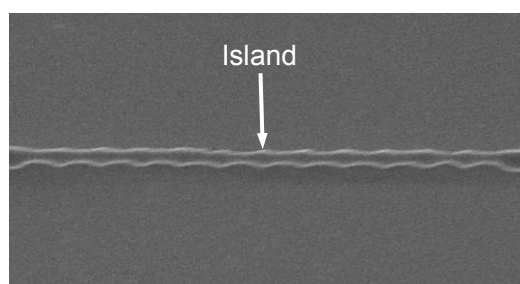


Fig. 4.4 A resist layer pattern of the multiple Coulomb Islands with nanowire barriers.

The top-silicon layer of the SOI was etched with the resist pattern as a mask using an ECR-etcher. The used gas was $\text{Cl}_2 = 40$ sccm. After the etching of the island array, subsequent isotropic wet etching in an $\text{NH}_4\text{OH}(28\%)/\text{H}_2\text{O}_2(50\%)/\text{H}_2\text{O}$ (=420 ml/180 ml/9 ml) solution for 30 min at 80 °C was carried out to reduce the dimensions of the array as shown in Fig. 4.5 [2]. Next, the oxidation was carried out to further reduce the size of the islands and the width of the nanowire barrier regions, which act as tunnel barriers for electrons. The nanowire regions (constricted region in the channel) act as a tunnel barrier due to the quantum-size effect. The final island size and wire width were about 50 nm and 30 nm, respectively. The final thickness of the top-silicon was about 18 nm. Si-SET biosensors have higher sensitivity than nanowire FET ones because of their Coulomb oscillations.

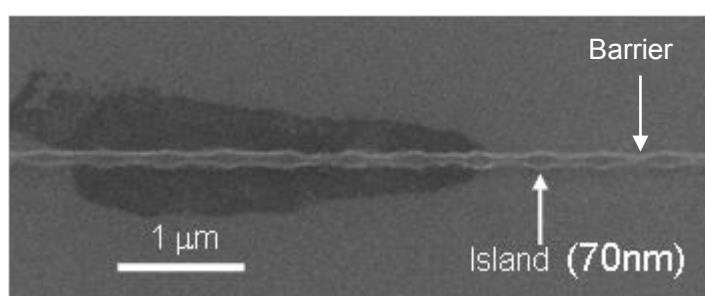


Fig. 4.5. Scanning electron micrograph of the multiple Coulomb Islands with nanowire barriers after dry and wet etching [2].

4.4. New Functional Gate MOSFET for Low Power

Here, as a device using silicon nanoscale structures, the functional gate MOSFET for low power logic operation is described [3, 4].

4.4.1. Principle of New Functional Gate MOSFET for low Power

A schematic diagram of fabricated n-channel MOSFET with a functional gate is shown in Fig. 4.6 The structure of the MOSFET resembles that of the conventional floating gate memory. The only difference is that a thin tunnel gate SiO_2 exists between the floating gate and the top gate electrode in the functional gate. Hereafter, the “the floating gate” in fabricated logic device is referred to as a “charge trap layer” in distinction from memory devices. In the MOSFET, electrons move between the charge trap layer and the top gate electrode through the tunnel gate oxide. The operation principle of the fabricated n-channel MOSFET and band diagram of the functional gate structure are shown in Fig. 4.7. Initially, no electrons move between the charge trap layer and the top gate electrode because of the charge neutrality in the charge trap layer when the gate voltage (V_g) is sufficiently low (usually $V_g = 0\text{V}$) in the off-state [Fig. 4.7(a)]. In this case, the off-state current (I_{off}) [in drain current (I_d)] is sufficiently low at the off-state voltage (V_{off}) [$V_g = 0\text{ V}$], as shown by curve A in Fig. 4.7(d). However, the on-state current (I_{on}) also becomes low at the on-state voltage (V_{on}) [curve A of Fig. 4.7(d)]. On the other hand, when V_g is switched to a large value in curve A, electrons move from the charge trap layer to the top gate electrode [Fig. 4.7(b)]. Since this leads to an additional lowering of the surface potential of the channel, the V_{th} shifts in the negative direction and I_{on} increases [curve B of Fig. 4.7(d)]. Finally, when V_g returns to a low value in curve B [Fig. 4.7(c)], electrons return from the top gate electrode to the charge trap layer as a result of lowering of the Fermi energy level caused by electron ejection. Therefore, the V_{th} changes back to the positive direction and I_{off} decreases [curve A of Fig. 4.7(d)]. In this way, the proposed MOSFET can increase I_{on} without increasing I_{off} , and this leads to ultralow power operation.

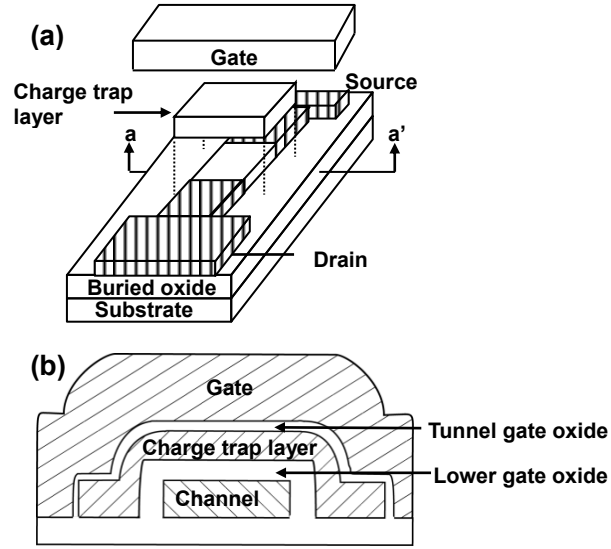


Fig. 4.6. (a) Schematic diagram of fabricated functional gate MOSFET. The shaded regions are heavily As^+ implanted. (b) Cross-sectional view along a–a' line in (a) [3].

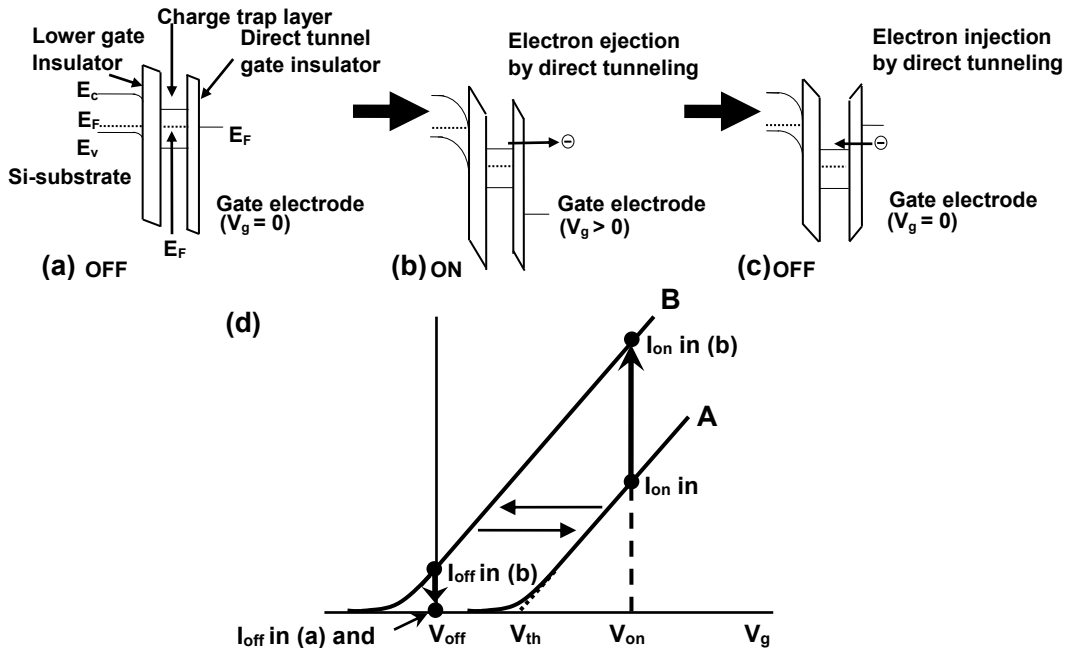


Fig. 4.7. Band diagrams of functional gate structure of the MOSFET in the off-current and on-current states (a) in the condition of charge neutrality in the charge trap layer, (b) in the case of electrons moving from the charge trap layer to the top gate electrode, (c) in the case of electrons returning from the gate electrode to the charge trap layer. (d) The operating principle of self-adjustment of the threshold voltage (V_{th}) for ultralow power operation of the proposed functional gate MOSFET. E_c , E_v , and E_F are the energies of conduction-band edge and valence-band edge, and Fermi energy level, respectively [3].

4.4.2. Device Structure and Fabrication Process

The structure of the proposed MOSFET resembled that of the conventional floating gate memory. The device fabrication process was similar to that of the floating gate memory previously reported [5-7] with a slight modification. Only the difference was that a thin tunnel gate SiO_2 existed between the floating gate and top gate electrode for the proposed functional gate. Electrons transferred between the floating gate and the top gate electrode in the proposed device. A p-type (B-doped) silicon-on-insulator (100) wafer was used. Electron beam lithography and dry etching were utilized to define the charge trap layer and channel. The thickness of the silicon channel was 60 nm. The channel width (W) and length (L) were changed as follows: $0.5\ \mu\text{m} \times 0.5\ \mu\text{m}$, $0.7\ \mu\text{m} \times 0.7\ \mu\text{m}$, $0.8\ \mu\text{m} \times 0.8\ \mu\text{m}$, $1.0\ \mu\text{m} \times 1.0\ \mu\text{m}$ and $1.0\ \mu\text{m} \times 18\ \mu\text{m}$, respectively. After defining the channel area and forming the lower gate oxide, an amorphous silicon film was deposited for the charge trap layer. Then, the resist mask line was formed parallel to the channel. Dry etching was carried out to define the width of the charge trap layer. The width of the charge trap layer was slightly larger than that of the channel. While the tunnel gate oxide was formed by thermal oxidation, the amorphous silicon of the charge trap layer changed to poly-silicon. After that, a poly-silicon film was deposited for the top gate electrode and doping of the poly-silicon was carried out by POCl_3 diffusion. Next, the resist mask line was formed perpendicularly across the channel. This time, the dry etching was stopped upon reaching the lower gate oxide. The lengths of the charge trap layer and the top gate electrode were made the same as that of the channel by using this self-aligned etching process. As for the thicknesses of the tunnel gate oxide (T_{ox}) were two types of 1.2 and 2.4 nm. The lower gate oxide is 10 nm. The thickness of the charge trap layer was 70 nm. After the source and drain areas were formed by ion implantation of As^+ at 30 keV with a dose of $4 \times 10^{15}\ \text{cm}^{-2}$ and annealing, the interlayer dielectrics were deposited. The device fabrication was completed with the formation of Ohmic contacts. The electrical characteristics were measured using a semiconductor

parameter analyzer with a pulse generator (4156 C and 41501B, Agilent). For the measurements, the electron injection into the charge trap layer was carried out by applying a negative bias V_g with 0V at the source while keeping the substrate and drain open. On the other hand, the electron ejection was carried out by applying a positive bias V_g with 0V at the source while keeping the substrate and drain open. I_d - V_g measurements were carried out immediately after electron injection or ejection. It took about 30 s for one I_d - V_g measurement.

4.4.3. Result

Figure 4.8 shows the dependence of drain current (I_d)- V_g characteristics on bias V_g application for the device with $T_{ox} = 1.2$ nm. In Fig. 4.8(a), V_{th} was measured after the positive bias V_g (which varied from 1 to 10 V with a voltage step of 1 V) was applied to the gate electrode for 60 s. While V_{th} shift did not occur until the positive bias voltage was 7 V, V_{th} shifted to the negative side above 8 V, which was the opposite direction to that of conventional floating gate memory, showing that the trapped electrons were indeed ejected from the charge trap layer. Owing to the relatively large T_{ox} , V_g over 8 V was necessary to eject electrons from the charge trap layer by direct tunneling for 60 s of V_g application time. When V_{th} was defined as V_g at an I_d of 10^{-7} A, the value of V_{th} shift was -0.15, -0.53, and -1.06 V for a V_g application of 8, 9, and 10 V, respectively. Here, V_{th} was returned to around the initial V_{th} value by the procedure described later before each V_g application and the V_{th} shift were measured from the returned value. For these V_g applications, effective voltage of 0.9–1.1 V is estimated to be applied to the tunnel gate oxide. Therefore, self-adjustment of V_{th} , which increased the on-current, was realized keeping the off-current low. By the application of negative V_g , V_{th} returned to close to the initial V_{th} value [Fig. 4.8(b)]. After the positive V_g application of 10 V for 60 s, the subsequent negative V_g application of -10 V for 60 s made V_{th} shift to the positive side, showing the electron injection into the charge trap layer. The direction of the V_{th}

shift was also opposite to that of conventional floating gate memory.

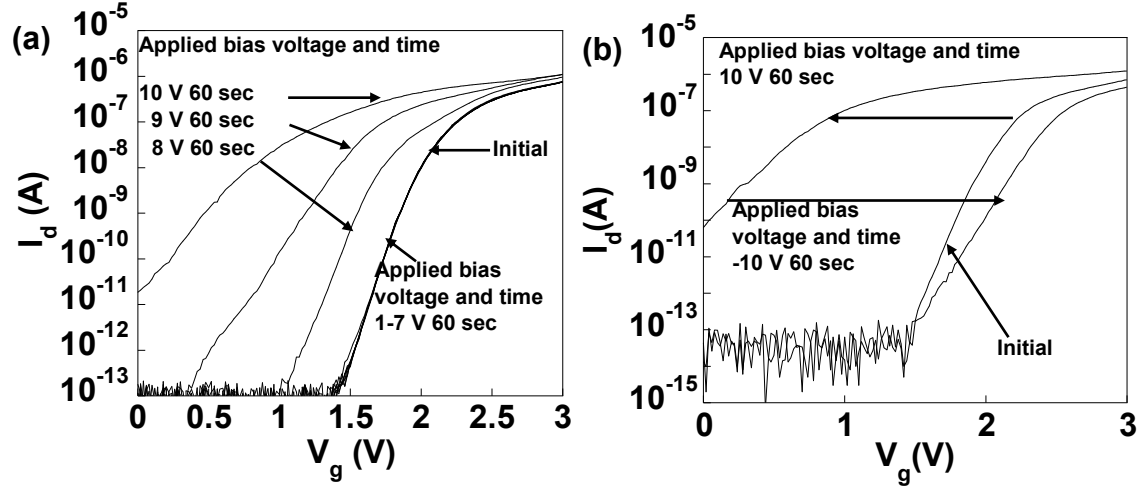


Fig. 4.8. Bias voltage dependence of I_d - V_g characteristics. $V_d = 0.1$ V. (a) After 60 s of application of positive bias V_g (1–10 V with 1 V steps) was applied, I_d - V_g curve was obtained. (b) I_d - V_g characteristics after positive bias V_g application (10 V, 60 s) and subsequent negative bias V_g application (-10 V, 60 s) [4].

Figure 4.9 shows I_d -drain voltage (V_d) characteristics after the positive and negative bias voltage applications. Typical I_d - V_d characteristics such as clear saturation were obtained after both the positive and negative V_g applications. Consistent with the results in Fig. 4.8, the on-current is indeed larger after the positive V_g application of 10 V for 60 s than after the subsequent negative V_g application of -10 V for 60 s.

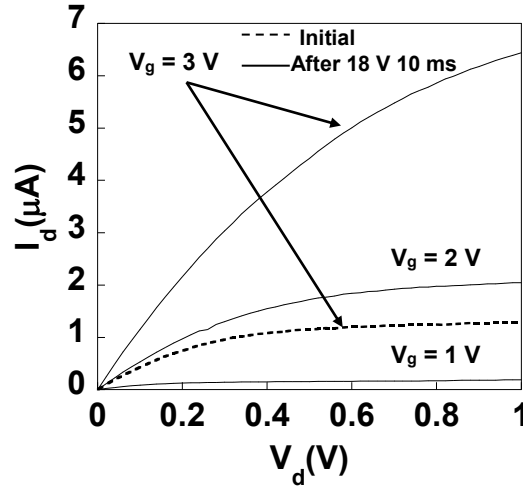


Fig. 4.9. I_d - V_d characteristics as a parameter of V_g after the positive bias V_g application (10 V, 60 s) (solid line) and subsequent negative bias V_g application (-10 V, 60 s) (broken line) [4].

Figure 4.10 shows the dependence of I_d - V_g characteristics on time after the application of positive V_g . After the V_g application, it was seen that V_{th} slowly returned to the initial V_{th} value; electron injection into the charge trap layer occurred slowly. The characteristic time was found to be over an hour. Although it took a long time to become off-current state, the off-current became sufficiently low. Strictly speaking, to use the proposed device for logic applications, quick recovery to the off-current state is necessary when V_g returns to 0 V from a high voltage. The way to make the time as short as 0.1 ns is to reduce T_{ox} to 0.5 nm. According to an extrapolation from the experimental data of electron tunneling injection/ejection [8], the time becomes as short as 0.1 ns when T_{ox} is reduced to 0.5 nm. Though it looks very difficult to realize such a thin T_{ox} , it will be possible utilizing techniques such as atomic layer deposition (ALD) [9-13]. Indeed, a thin (physical thickness of 0.5 nm) silicon nitride was successfully deposited on a silicon substrate by ALD as a barrier layer of ZrO_2 gate dielectrics [12, 13]. For a thin tunnel oxide with $T_{ox} = 0.5$ nm, tunnel current density is simulated to be about 10^5 A/cm² at a gate voltage of 0.5 V for an n⁺-gate/p-silicon nMOSFET [14]. Using the tunnel current density, the injected/ejected charge amount ΔQ to/from the

charge trap layer is 10^{-5} C/cm^2 during a switching time of 0.1 nm. Then, the threshold voltage shift ΔV_{th} accompanied with the charge injection/ejection is calculated to be 1.4 V from $\Delta V_{th} = \Delta Q/C$. Here, the capacitance C between the upper gate and the charge trap layer is $6.9 \times 10^{-6} \text{ F/cm}^2$ since the upper gate oxide is the tunnel gate oxide ($T_{ox} = 0.5 \text{ nm}$) for the device in this study. Therefore, sufficient ΔV_{th} is considered to be obtained at $T_{ox} = 0.5 \text{ nm}$ for the ultralow power logic application. It should be noted that, as far as for the ultralow power logic applications to such as watches, health care devices, or passive radio frequency integrated circuit tags, the relatively long characteristic time may be allowable and T_{ox} can be much larger than 0.5 nm.

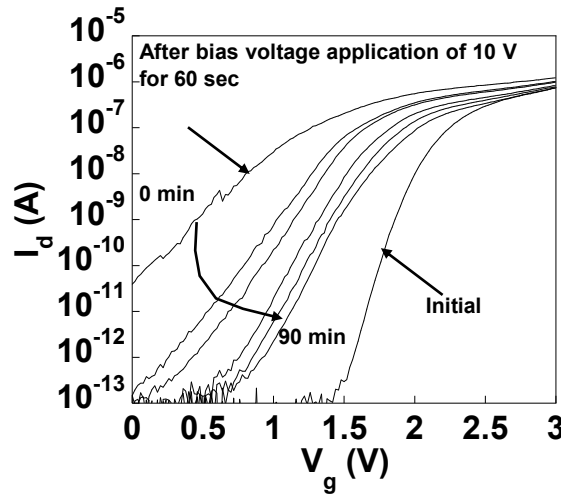


Fig. 4.10. Time dependence of I_d - V_g characteristics after the positive bias V_g application (10 V, 60 s) [4].

I_d - V_g curves were measured at 0, 5, 10, 30, 60, and 90 min after the V_g application. $V_d = 0.1 \text{ V}$.

Next, the electrical characteristics for the device with $T_{ox} = 2.4 \text{ nm}$ were measured. Compared with the previous ones for the device with $T_{ox} = 1.2 \text{ nm}$, the large V_g with short time was applied for quick device operation. Figure 4.11(a) shows the I_d - V_g characteristics for positive and negative bias V_g applications. Since it is important to evaluate the change of the required gate voltage in the on-current state, I_{onc} was defined as I_d at the V_{th} plus 1.0V and V_{onc} was defined as V_g at I_{onc} . Accordingly, I_{onc} was $3.7 \mu\text{A}$ and V_{onc} was 4.3V in the initial I_d - V_g characteristics. Note that

the gate leakage current ($I_{\text{g leak}}$) was less than the noise level (1 pA) in the V_g range from 0 to 10V (not shown). After a positive bias V_g of 18V was applied for 10 ms, V_{onc} shifted to the negative side of the initial V_{onc} value, indicating that electrons were ejected from the charge trap layer. Note that the direction of the V_{onc} shift was opposite to that of conventional floating gate memories. A subsequent negative bias V_g application of -10V for 10 ms made V_{onc} return to a value close to the initial V_{onc} , indicating that electrons were injected into the charge trap layer. Here, the shift in V_{onc} (ΔV_{onc}) was about -0.25 and 0.22V after positive and negative bias V_g applications, respectively. These results prove the feasibility of the operation principle of the fabricated MOSFET with a functional gate, which increases I_{on} without increasing I_{off} . In Fig. 4.11(b), the ordinate axis for I_d is a log scale. Although the reason is not clear yet, the shift in V_g for a constant I_d in the small I_d region ($I_d < 0.5 \mu\text{A}$) was larger than in the large I_d region ($I_d > 0.5 \mu\text{A}$) after the positive and negative bias V_g applications.

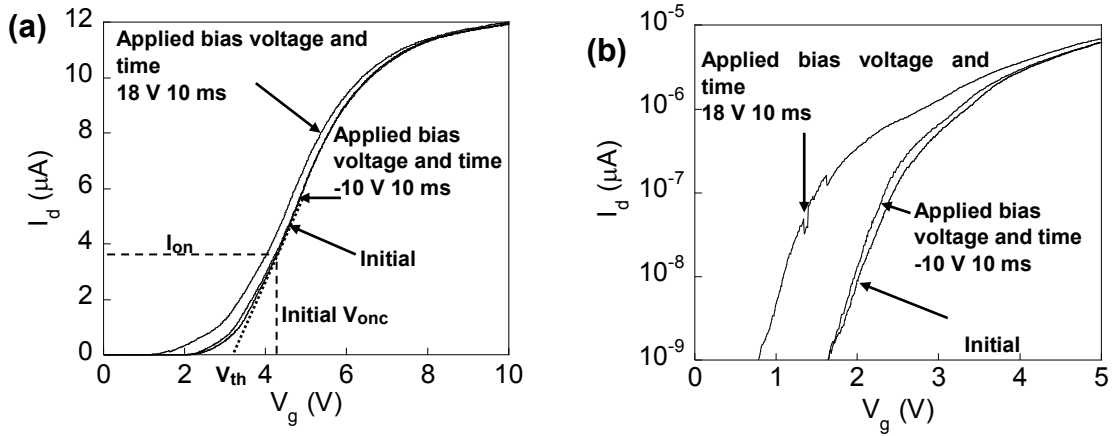


Fig. 4.11. Bias voltage dependence of drain current (I_d)-gate voltage (V_g) characteristics. Drain voltage (V_d) = 0.1 V. (a) Initial I_d - V_g characteristics and those after a positive bias V_g application (18 V, 10 ms) and those after a subsequent negative bias V_g application (-10 V, 10 ms). The dotted line illustrates the linearly extrapolated threshold voltage (V_{th}) at the initial I_d - V_g characteristics. Broken lines indicate I_{onc} (defined as I_d at the V_{th} plus 1.0 V) and V_{onc} (defined as V_g at I_{onc}) at the initial I_d - V_g characteristics. (b) Note that the linear scale axis of I_d in (a) has been changed to a log scale in this figure [3].

Figure 4.12 shows the dependence of I_d on the drain voltage (V_d) before and after applying a positive bias V_g of 18V for 10 ms. The device showed typical I_d – V_d characteristics, such as clear I_d saturation at $V_g = 3\text{V}$, before and after the positive bias. Consistent with the results in Fig. 4.11, I_{on} was indeed larger after the positive bias.

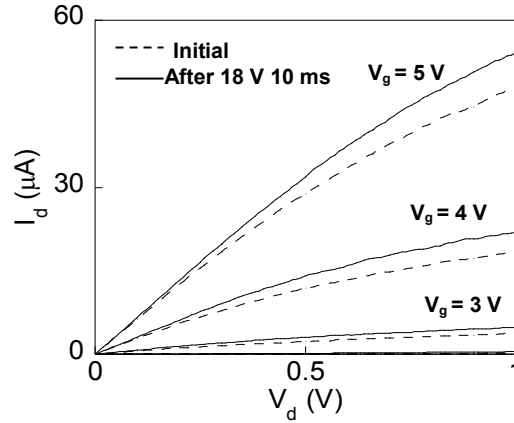


Fig. 4.12. Drain current (I_d)–drain voltage (V_d) characteristics as a parameter of gate voltage (V_g) before (broken line) and after (solid line) positive bias V_g application (18 V, 10 ms) [3].

Figure 4.13(a) shows the I_d – V_g characteristics when a negative bias was not applied after the positive bias. Here, the initial I_{onc} was $3.9\ \mu\text{A}$ and V_{onc} was 4.3V in the initial I_d – V_g characteristics. The first I_d – V_g measurement was carried out immediately after a positive bias V_g of 18V was applied for 10 ms. The initial V_{onc} shifted in the negative direction (ΔV_{onc} was -0.3 V). The second I_d – V_g measurement was carried out immediately after the first one. In this case, V_{onc} changed to the positive direction and returned to a value close to the initial one (the voltage difference between initial V_{onc} and this V_{onc} was slight, 0.03 V). Since it took about 30 s for each I_d – V_g measurement, the time necessary for V_{onc} to return to the initial value ranged from about 30 to 60 s. Figure 4.13(b) shows the endurance characteristic of this device. Here, V_{low} and V_{high} are defined as the V_{onc} for the first and second I_d – V_g measurements after the positive bias at each cycle, respectively. Both V_{high} and V_{low} increased with the cycle number. As described later, this increase is mainly caused by electrons that get trapped in the lower gate oxide during the positive bias V_g applications.

However, as shown in Fig. 4.13(c), the voltage difference between V_{high} and V_{low} remained approximately constant (almost the initial value of 0.3 V) even after 10^5 cycles of electron ejection and injection.

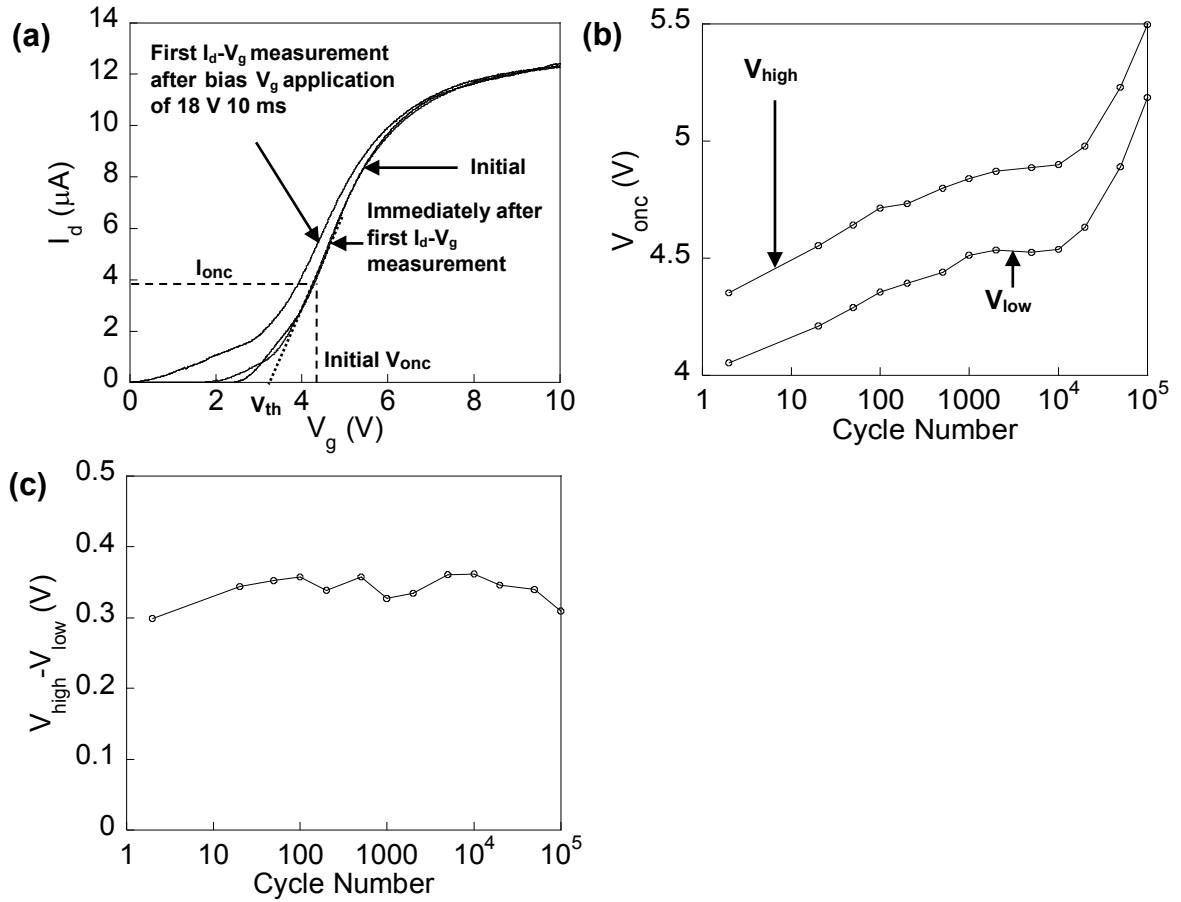


Fig. 4.13. (a) Initial drain current (I_d)-gate voltage (V_g) characteristics and those of the first measurement after a positive bias V_g application (18 V, 10 ms). Immediately after the first I_d - V_g measurement, the I_d - V_g characteristics were measured again. The dotted line illustrates the linearly extrapolated threshold voltage (V_{th}) at the initial I_d - V_g characteristics. Broken lines also indicate I_{onc} (defined as I_d at the V_{th} plus 1.0 V) and V_{onc} (defined as V_g at I_{onc}) at the initial I_d - V_g characteristics. (b) Endurance characteristics of the tunnel and lower gate oxides. V_{low} is V_{onc} for the measurement after the positive bias V_g application (18 V, 10 ms) and V_{high} is V_{onc} for the measurement before the positive bias V_g application. The measurement of V_{low} and V_{high} was carried out at 2, 20, 50, 100, 200, 500, 1000, 2000, 5000, 10 000, 20000, 50 000, and 100 000 cycles. (c) Dependence of the voltage difference between V_{high} and V_{low} in (b) on the cycle number. The device used in the measurement in Fig. 4.13 is different from that in Fig. 4.11 [3].

Figure 4.14 shows the dependence of the oxide breakdown characteristics on the size of the channel region. The widths (W) x lengths (L) of the channels were $0.5\ \mu\text{m} \times 0.5\ \mu\text{m}$, $0.7\ \mu\text{m} \times 0.7\ \mu\text{m}$, and $1.0\ \mu\text{m} \times 1.0\ \mu\text{m}$. The initial V_{onc} values were 4.7, 5.0, and 5.3V for the respective devices. The applied values of positive and negative biases were 15.4 and -6.0 V, 15.7 and -5.7 V, and 16.0 and -5.6 V, respectively. To make the number of transferred electrons almost the same in injection and ejection, the positive and negative biases were set so that the absolute values of the difference between the initial V_{onc} and the positive bias were equal to that between the initial V_{onc} and the negative bias. In the endurance measurement, a large I_{gleak} eventually flowed from the gate electrode to the source/drain electrodes through the channels. This indicates that breakdown occurred in both the tunnel and lower gate oxides.

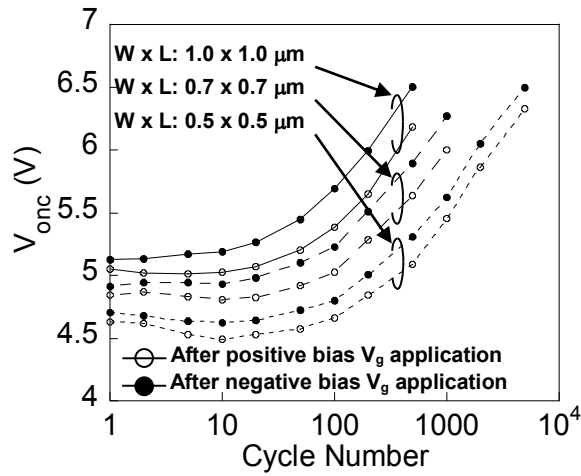


Fig. 4.14. Dependence of oxide breakdown characteristics on the channel size. V_{low} and V_{high} are the V_{onc} after positive and negative bias V_g applications, respectively. V_{low} and V_{high} were measured at 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000, 2000, and 5000 cycles [3].

Figure 4.15 shows the dependence on the channel size of the cycle number at which both the tunnel and lower gate oxides broke down. The figure shows results for a device with a channel size of $0.8\ \mu\text{m} \times 0.8\ \mu\text{m}$ in addition to those from Fig. 4.14. Breakdown occurred at 7753, 2273, 809,

and 605 cycles for the respective channel sizes of $0.5\ \mu\text{m} \times 0.5\ \mu\text{m}$, $0.7\ \mu\text{m} \times 0.7\ \mu\text{m}$, $0.8\ \mu\text{m} \times 0.8\ \mu\text{m}$, and $1.0\ \mu\text{m} \times 1.0\ \mu\text{m}$. This clearly shows that the cycle number at oxide breakdown increases as the channel size decreases. Therefore, the smaller the channel is, the less often breakdown occurs, meaning that electron traps randomly form in the oxide.

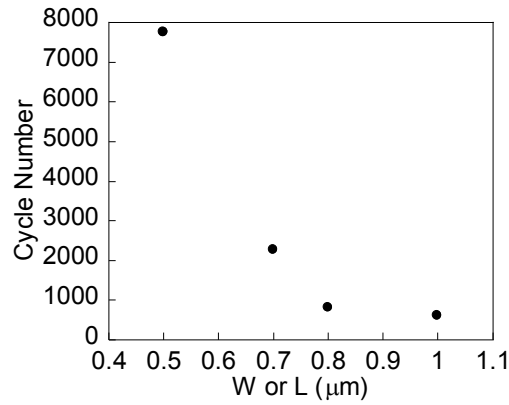


Fig. 4.15. Dependence on the channel size of the cycle number at which the breakdown of both the tunnel and lower gate oxides occurred [3].

4.4.4. Discussion

Figure 4.16 shows the dependence on the channel size of the voltage difference between V_{onc} after a positive bias V_g application (V_{low}) and after a subsequent negative bias V_g application (V_{high}). Here too, the results for a device with a channel size of $0.8\ \mu\text{m} \times 0.8\ \mu\text{m}$ have been added. The value of $V_{\text{high}} - V_{\text{low}}$ remained approximately constant after 100 cycles, especially for two devices ($W \times L$: $0.5\ \mu\text{m} \times 0.5\ \mu\text{m}$ and $1.0\ \mu\text{m} \times 1.0\ \mu\text{m}$). The tendency in the other two devices was to be constant, as well. Therefore, the difference between the number of injected and ejected electrons after 100 cycles is considered to be slight.

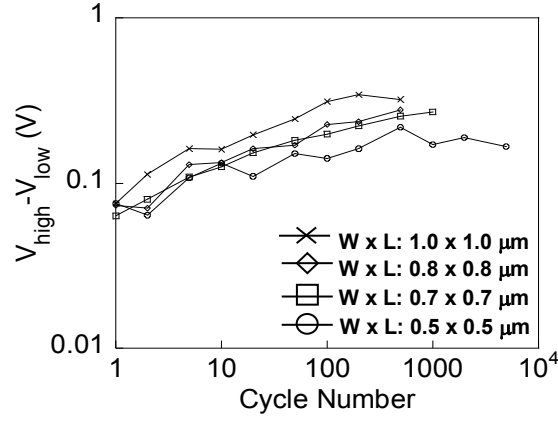


Fig. 4.16. Dependence of the voltage difference between V_{high} and V_{low} on the cycle number for different channel sizes [3].

The endurance characteristics of the devices were analyzed in order to clarify the breakdown mechanism of the tunnel and lower gate oxides. Figure 4.17 shows the breakdown characteristics of the gate oxide for two different devices fabricated on the same wafer as a function of the number of cycles of positive and negative bias V_g applications. Here, the negative bias was applied in order for high speed injection of electrons into the charge trap layer. The two devices had the same structure and channel size ($L = 0.5 \mu\text{m}$, $W = 0.5 \mu\text{m}$) and thicknesses of tunnel and lower gate oxides. One device, which is referred to as “type A” hereafter, kept an approximately constant $V_{\text{high}} - V_{\text{low}}$ during the positive and negative bias V_g applications above 5000 cycles [Fig. 4.17(a)]. After 5000 cycles, oxide breakdown was accompanied by a large I_{leak} , indicating both tunnel and lower gate oxides broke down. In contrast, the other device, which is referred to as “type B” hereafter, $V_{\text{high}} - V_{\text{low}}$ gradually decreased as the cycle number increased and this window eventually closed [Fig. 4.17(b)]. The difference between V_{high} and V_{low} at around 104 cycles was 0.02 V, whereas the initial value was 0.12 V. I_{leak} was still smaller than the noise level at around 104 cycles. As described below, the tunnel gate oxide would have broken down immediately after the lower gate

oxide broke down, leading to a large $I_{\text{g leak}}$. Therefore, it was considered that the lower gate oxide did not break down in this device. Note that the number of fabricated devices showing type-A characteristics was much larger than those showing type-B characteristics.

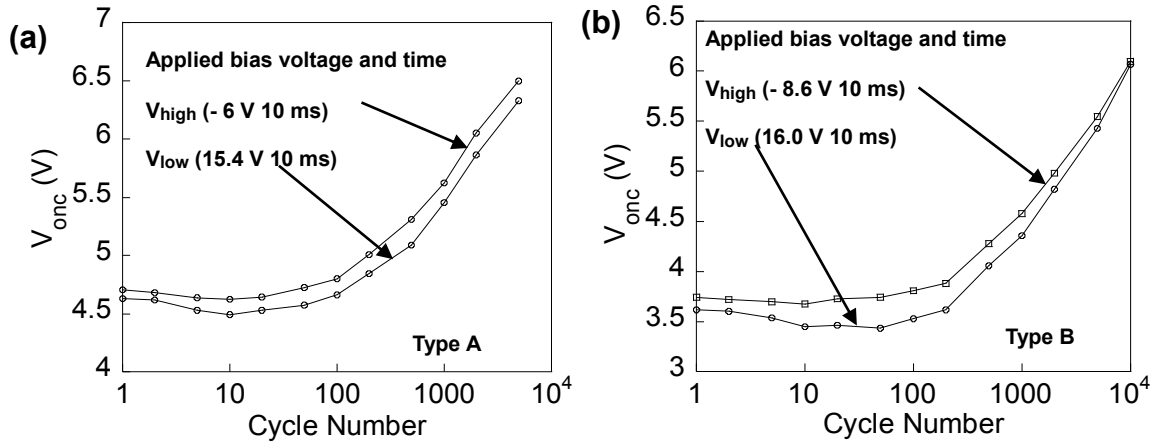


Fig. 4.17. Two types of oxide breakdown [(a) type A and (b) type B] as a function of cycles of positive and negative bias V_g applications. (a) V_{low} and V_{high} are V_{ox} after positive (15.4 V) and negative (-6.0 V) bias V_g applications (10 ms). (b) V_{low} and V_{high} are, respectively, V_{ox} after positive (16.0 V) and negative (-8.6 V) bias V_g applications (10 ms). V_{low} and V_{high} were measured at 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000, 2000, and 5000 cycles [3].

It was considered that these two types of device have different oxide deterioration and breakdown mechanisms. In particular, the lower gate oxide must have broken down in the type A devices since a large leakage gate current was detected. Once that occurred, the whole V_g was applied only to the remaining thin tunnel gate oxide and the electric field in the tunnel gate oxide increased to an extremely high value. Was I to assume that oxide breakdown does not occur in the tunnel oxide, the electric field would be 64 MV/cm. This value is much larger than the breakdown fields of typical oxides, around 10 MV/cm [15] and this means the tunnel gate oxide must have immediately broken down after the lower gate did.

The thickness of the lower gate oxide was 10 nm, and it is well known that a percolation

model accurately explains how oxides with such thicknesses break down [16–18]. In reference to our results, application of the bias V_g caused a high electric field at the lower gate oxide and this generated electron traps. According to the percolation model, the electron traps that were generated in the lower gate oxide became connected and acted as a conductive path from the charge trap layer to the channel. This led to breakdown of the lower gate oxide. Indeed, the increase in V_{high} and V_{low} after 10 cycles in the type-A device [Fig. 4.17(a)] is considered to have been caused by an increase in the trapped electrons in traps generated in the lower gate oxide.

On the other hand, lower gate oxide did not break down in the type-B devices. The gradual closing of the window between V_{high} and V_{low} with the cycle number can be explained as follows [19]. Besides the increase in the trapped electrons in the lower gate oxide, the number of trapped electrons in the tunnel gate oxide gradually increased with the cycle number. These trapped electrons decreased the tunnel efficiency through the tunnel gate oxide during the negative and positive V_g biases. This led to a decrease in the number of electrons injected into the charge trap layer through the tunnel gate oxide during a negative bias, which resulted in a decrease in V_{high} . Similarly, the number of electrons ejected from the charge trap layer decreased as a result of the decrease in tunnel efficiency through the tunnel gate oxide during the positive bias V_g application. This helped to increase V_{low} . The decrease in V_{high} and increase in V_{low} caused the window of $V_{high} - V_{low}$ to close. Note that besides the above effects on V_{th} , there was also a base increase in V_{th} caused by the trapped electrons in the lower gate oxide, as described before in the discussion of type A. Combining this base increase effect with the above effect, I can see that the rise in V_{low} becomes much sharper compared with the rise in V_{high} [see Fig. 4.17(b)]. The window did not close when the breakdown of the lower gate oxide occurred before 104 cycles. Therefore, the window closing would have appeared in most of the devices if the lower gate oxide did not break down after 104 cycles.

Next, the reason for the dependence of the breakdown characteristics on the channel size

will be discussed by using the percolation model [16–18]. As shown in Fig. 4.15, the smaller the channel is, the less often breakdown occurs. The breakdown of the lower gate oxide is caused by the generated electron traps connecting the charge trap layer and the channel. Only one such conductive path is enough to cause the lower gate oxide to break down. Since the electron traps are distributed randomly in the lower gate oxide, the probability of forming one conductive path becomes larger as the channel size increases. Therefore, the endurance characteristics of the oxide improve as the channel size decreases.

Then, let us discuss the way to increase the operation speed of our device. It took somewhat long for the fabricated device to return to the off-current state from a high voltage, as shown in Fig. 4.13(a). Strictly speaking, use of the proposed device in logic applications would necessitate a quicker recovery to the off-current state. The conventional CMOS logic used in personal computers operates at a few gigahertz, and advanced logic applications require the operation frequencies over 10 GHz, which corresponds to an operation time of 0.1 ns. In the fabricated device, one of the ways to make the operation time as short as 0.1 ns is to reduce T_{ox} to 0.5 nm. According to an extrapolation from the experimental data of electron tunneling injection and ejection [13], the operation time is as short as 0.1 ns when T_{ox} is 0.5 nm with bias V_g application. Though such a thin T_{ox} seems very difficult to realize, it will soon be possible by utilizing techniques such as atomic layer deposition (ALD) [9, 21–23]. Indeed, a thin (physical thickness of 0.5 nm) silicon nitride was successfully deposited on a silicon substrate by ALD as a barrier layer of ZrO_2 gate dielectrics [13, 23]. Even if such an ultimate deposition technique is not used, our device would still have applications that normally operate at a lower frequency. In particular, the relatively long characteristic time would not necessarily be a problem in ultralow power applications for watches, health care devices, and passive radio frequency integrated circuit tags.

Furthermore, the decrease in the thickness of the tunnel gate oxide will lead to a decrease

in the power-delay product (PDP) due to the shorter electron ejection time from the charge trap layer. As mentioned before, the operation time of our device can be reduced to about 0.1 ns for a thickness of 0.5 nm. With a drain current of 10 μ A and drain voltage of 0.1 V, the PDP becomes about 0.1 fJ, which is smaller than that of present logic operations whose order ranges from fJ to pJ.

With continued device scaling, fluctuations in V_{th} may become relatively large and be a problem for proper logic operations. One solution is to use the verify process which makes the V_{th} shift uniform among devices. In flash memory, it takes about 200 μ s for a whole program/verify process. For logic circuits, the operation time seems to be too long; however, the verify process can be used in some ultralow power logic applications, such as watches whose typical operation time is 1 s. From the viewpoint of fabrication, on the other hand, separating the charge trap layer to multiple parts or increasing the number of the charge trap layer is one idea to make V_{th} shift uniform. Even if the size of each trap layer varies, the size distribution in the trap layers will be similar, and this will reduce the V_{th} variation among the devices. Another idea is to reduce the thickness variation of the tunnel oxide by using the techniques such as ALD. Such a reduction would enable the variation in the number of injected and ejected electrons to be reduced, which makes V_{th} shift uniform among devices. If I can reduce the variation of V_{th} shift among devices to some extent by using the above fabrication processes, I can further reduce the whole time for the verify process.

Finally, it should be noted that for reliability enhancement, making the floating gates plural may be effective. Separating the trap charge layers into plural ones could effectively avoid the V_{th} shift caused by the production of a leakage pass as can be seen in the case of floating dot memory [22, 23].

Therefore, it should be noted that while our devices showed the self-adjustment of V_{th} due to the relatively thick tunnel oxide in this study, the positive bias V_g necessary for the electron ejection from the charge trap layer can be much decreased by reducing the thickness of the tunnel

gate oxide. In this case, since electron ejection leads to a sharp rise in I_d when the device is switched from the off-state to the on-state, small S-factors can appear. When the device is switched from the on-state to the off-state, on the other hand, electrons are injected to the charge trap layer, which also results in a decrease in the S-factor. This would enable us to increase the on-current without increasing the off-current for ultralow power operation.

4.4.5. Summary

A functional gate MOSFET was devised and its operating principle, which enables the on-current to be increased without increasing the off-current for ultralow power operation was demonstrated. The systematic study of the fundamental device characteristics necessary for ultralow power operation was demonstrated putting emphasis on the device reliability. A negative V_{th} shift was caused by electron ejection, and a positive V_{th} shift was caused by electron injection. The measured endurance characteristics of the tunnel and lower gate oxides indicated that oxide breakdown did not occur until 10^5 electron ejection-and-injection cycles when only a positive bias V_g was applied. Endurance characteristics showed that the number of cycles to breakdown increases as the channel size decreases. Two different oxide breakdown characteristics were found. In one type, both the lower and tunnel gate oxides broke down. In the other, the window between V_{high} and V_{low} closed before oxide breakdown occurred. These oxide breakdown mechanisms were explained with a percolation model. Since a smaller channel greatly improves the endurance characteristics and the decrease in T_{ox} leads to high-operation speed, the scaling down of the device will open the way to the development of CMOS logic applications for it in the sub-32nm technology node.

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Chapter 5 pH Sensor and Biosensor Using Silicon nanowire

FET with Thin Gate Insulator

Here, as devices using silicon nanoscale structures, pH sensors and biosensors using silicon nanowire FET (SiNW- FET) with thin gate insulator are described [1, 2].

5.1. Advantage of pH Sensor and Biosensor Using Silicon nanowire FET with Thin Gate Insulator.

$\text{Si}_3\text{N}_4/\text{SiO}_2$ stack gate was used in pH sensor and biosensor because of the presence of the leakage path through the SiO_2 layer. However, if the thick $\text{Si}_3\text{N}_4/\text{SiO}_2$ gate insulator exists between channel and targets, the influence of target's charge decreases since the length between the channel and target becomes long. Therefore, sensors having a thinner Si_3N_4 gate insulator (the thickness are about 42 nm $\text{Si}_3\text{N}_4/10$ nm SiO_2 for ion sensor and 19 nm $\text{Si}_3\text{N}_4/8$ nm SiO_2 for biosensor) structure compared with that of the previous works (approximately Si_3N_4 100nm/ 100nm SiO_2) were fabricated, which lead to higher sensitivity in ion and biomolecule detection without reliability degradation.

5.2. Device Structure and Fabrication Process

An n-channel SiNW-FET on a silicon-on-insulator (SOI) wafer was fabricated using standard semiconductor technology. The thicknesses of the top Si layer (p-type, $10 \Omega\cdot\text{cm}$) and buried oxide layer of the SOI were 72 - 76 nm and 400 nm, respectively. The fabrication procedure was as follows.

(1) The thickness of the top Si layer of the SOI wafer was reduced to 30 nm by oxidation at 1000 °C.

- (2) The SiO_2 on the top Si layer of the SOI was removed by wet-etching.
- (3) A mask pattern of the SiNW was formed by electronbeam lithography with a negative resist (SAL-SR2). The top Si layer of the SOI was etched with the mask pattern using an electron cyclotron resonance etcher. Figure 3.1 shows a scanning electron micrograph of the fabricated structure after etching. The dimensions of the SiNW were approximately 5 mm x 80 nm x 17 nm (length x width x height).
- (4) The source and drain areas were formed by ion implantation of As^+ at 20 keV with a dose of $5 \times 10^{14} \text{ cm}^{-2}$.
- (5) Stacked gate insulators were fabricated by two procedures. SiO_2 with a thickness of 10 nm was thermally grown at 850 °C in a dry atmosphere followed by the deposition of 42 nm thick Si_3N_4 by low-pressure chemical vapor deposition at 750 °C for pH measurement. In addition, we fabricated another device with thin gate insulator (19 nm Si_3N_4 /8 nm SiO_2) for monitoring protein charge.
- (6) After wet-etching to form contact holes, Al electrodes were formed and postmetallization annealing was carried out at 400 °C under a hydrogen atmosphere for 30 min.

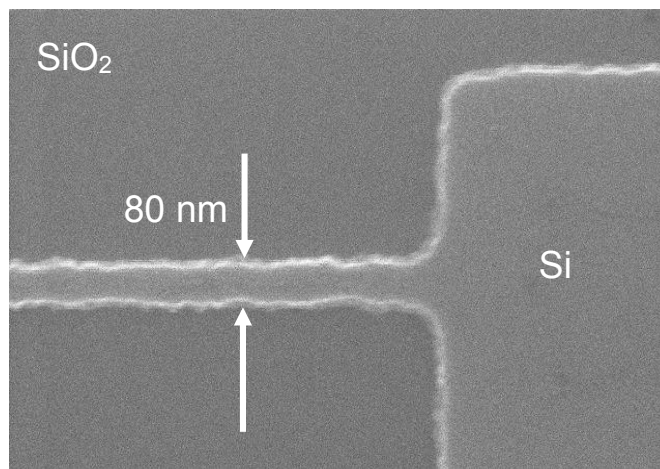


Fig. 5.1. Scanning electron micrograph of fabricated silicon nanowire (width: 80 nm) [1].

5.3. Schematic Diagram of Measurement System

Figure 3.2 shows a schematic diagram of our measurement system. A fluidic channel was made of poly(dimethylsiloxane) (PDMS). The volume of the cell was as follows: the size of the fluidic channel on the FET was approximately 3mm x 1mm x 100 mm (length x width x height). The whole area of the FET including the Al pad electrodes (1.0 mm²) was 33.0 mm². The joining surface of the fluidic channel was modified by O₂-plasma treatment, and then attached to the SiNW-FET. An Ag/AgCl reference electrode was used to control the gate voltage of the SiNW-FET through a buffer solution. The electrical characteristics were measured using a semiconductor parameter analyzer (Agilent B1500A).

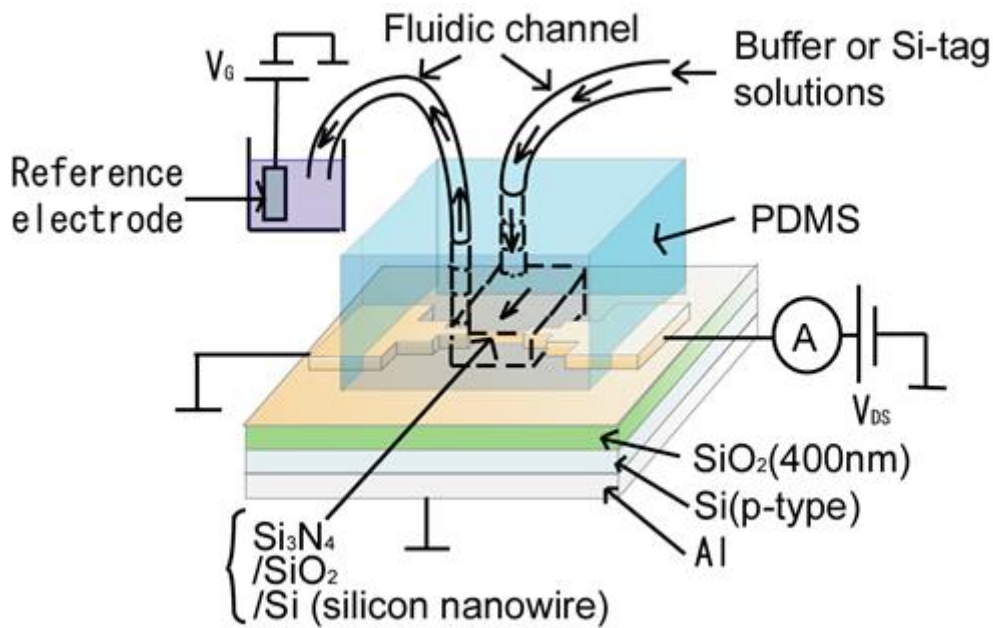


Fig. 5.2. Schematic diagram of measurement system [1].

5.4. pH Measurement

First, I investigated the electrical characteristics of the fabricated SiNW-FET in the presence of buffer solutions of different pH on the Si₃N₄ gate insulator. The measurement sequence

is shown in Fig 5.4.

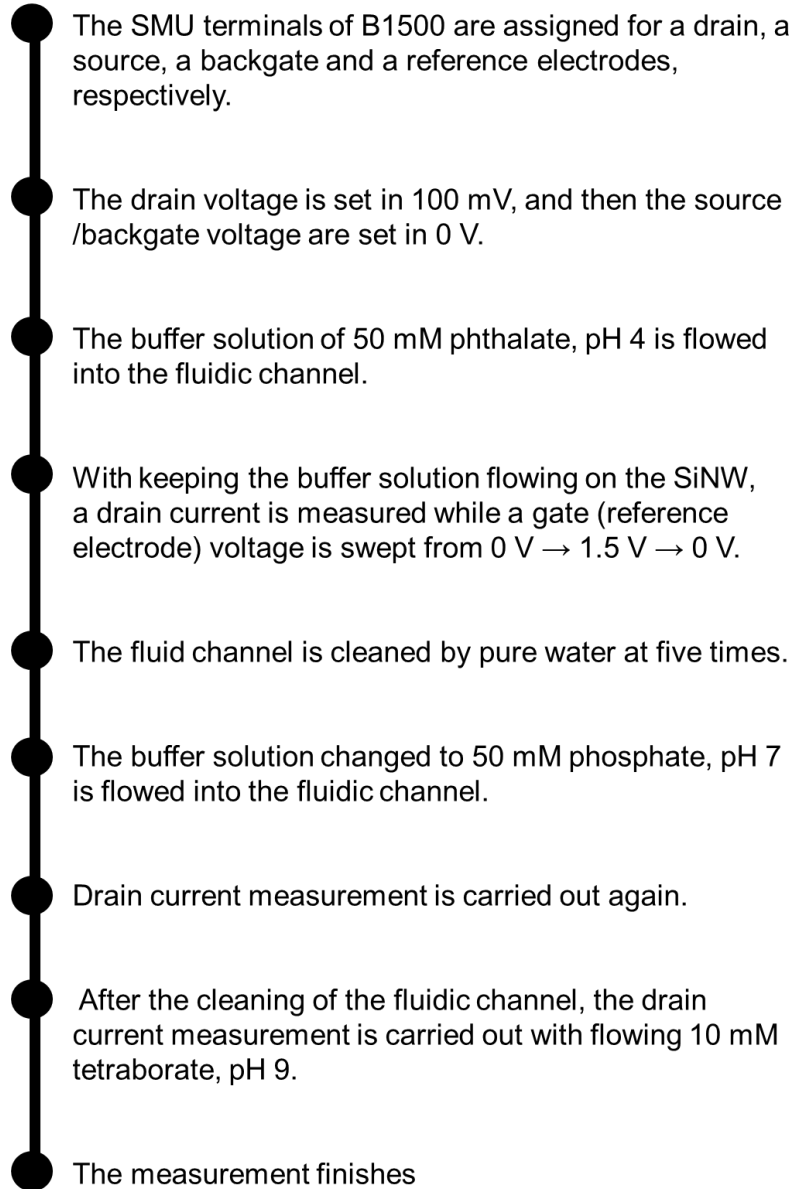


Fig. 5.4. Measurement sequence of I_d - V_g characteristics.

Figure 5.5 shows the drain current (I_{DS}) versus gate voltage (V_G) characteristics obtained in the forward and reverse sweeps. The drain - source voltage (V_{DS}) was fixed at 100 mV. The following three solutions were used: 10 mM tetraborate, pH 9; 50 mM phosphate, pH 7; and 50 mM

phthalate, pH 4. The threshold voltage was shifted in the positive (negative) direction with increasing (decreasing) pH of the solution with a shift of 60 mV/pH, which is in good agreement not only with the theoretical value (58 mV/pH, 20 °C) obtained using the Nernst equation but also with previous experimental results (46 - 56 mV/pH) [3,4]. In addition, the hysteresis was extremely small.

The pH response of the I_{DS} of the SiNW FET at a fixed V_G is shown in Fig. 5.6. The flow rate was 25 ml/min. When the buffer solution was changed from pH 7 \rightarrow 4 \rightarrow 7 (pH 7 \rightarrow 9 \rightarrow 7), the I_{DS} at a V_{DS} of 100mV and a V_G of 800 mV increased (decreased) in response to pH. The response time was 400 to 800 s. The changes in the I_{DS} were accurately reproduced. These results show that the fabricated SiNW FET has reproducibility of pH response and the capacity to detect changes in Si_3N_4 surface potential.

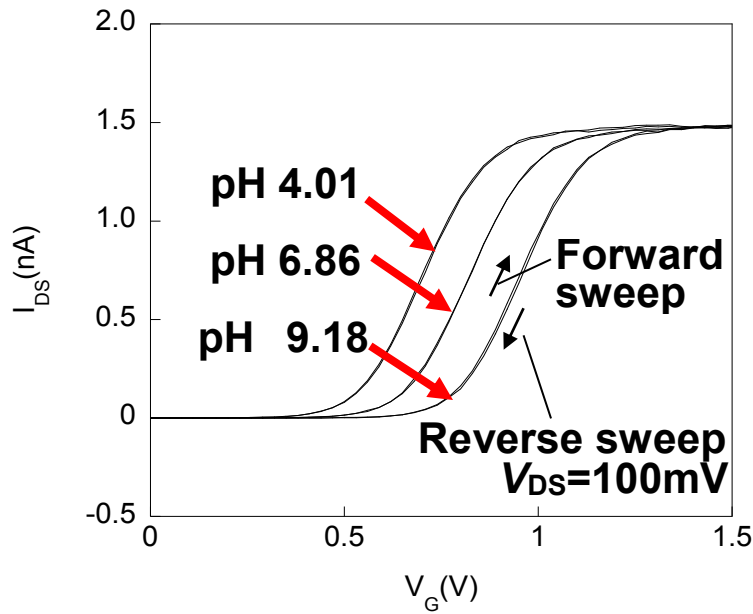


Fig. 5.5. Drain–source current (I_{DS}) vs gate voltage (V_G) characteristics of Si nanowire field-effect transistor in presence of three buffer solutions on the gate insulator surface. The drain–source voltage (V_{DS}) was fixed at 100 mV [1].

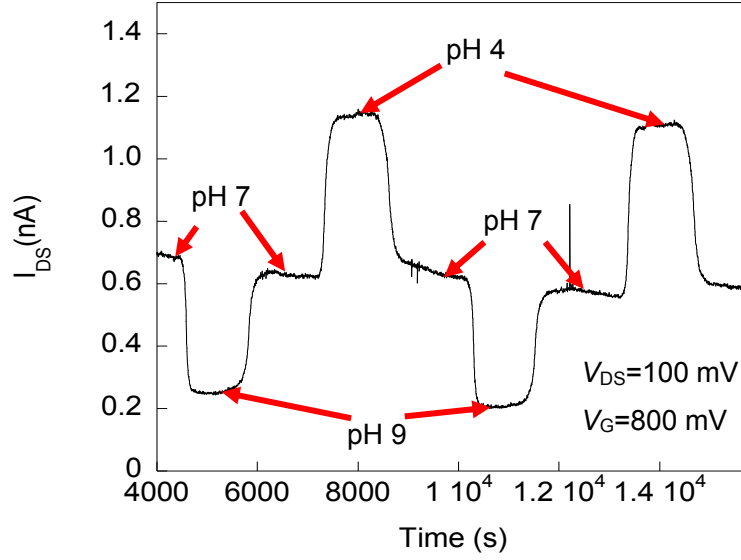


Fig. 5.6. Change over time of drain–source current (I_{DS}) during sequential injection of three buffer solutions of different pH. The drain–source voltage (V_{DS}) and gate voltage (V_G) were fixed at 100 and 800 mV, respectively [1].

5.5. Biomolecule Detection

The response of the SiNW-FET to electrical charges of a protein in solution was investigated. Si-tags, which are highly positively charged proteins, as a sample was used. For detection of charged molecules by FET, the Debye length should be longer than the size of the target; otherwise, counter ions in the solution shield the charge of the target. The Debye length b is given by

$$b = \left(\frac{e^2}{\epsilon_0 \epsilon_r k T} \sum_i n_i z_i \right)^{-1/2}$$

where e is the elementary electric charge, ϵ_0 and ϵ_r are the vacuum permittivity and relative permittivity of water, respectively, k is the Boltzmann constant, and T is the absolute temperature of the system. n_i and z_i are the concentration and charge of the primary ion i in the solution, respectively. In this study, I prepared the Si-tag solution (30 nM Si-tag in 20 ml of 1 mM tetraborate

buffer, pH 9), in which each Si-tag molecule had a positive charge of about $+30e$. Using the above equation, the Debye length of this solution is calculated to be about 7 nm. Since the size of each Si-tag is estimated to be about 3 nm, the Si-tags immobilized on the Si_3N_4 surface of a FET were within the Debye length. Figure 3.5 shows the change over time of I_{DS} at a V_{DS} of 100 mV and a V_G of 400 mV during successive introduction of the buffer solution, the Si-tag solution, and the buffer solution into the microfluidic channel. First, only the tetraborate buffer was injected into the microfluidic channel, and then, the Si-tags dissolved in tetraborate buffer were injected. When the Si-tags arrived at the SiNW, the drain current increased. The response time was about 50 s. While the Si-tags were flowing along the fluidic channel, the drain current stayed an increased current level because the positive charge of the Si-tags reduced the surface electric potential. The amplitude drift was about 25 mV while the Si-tags were flowing along the SiNW. This result indicates that the distance between the Si-tags and the Si_3N_4 surface was smaller than the Debye length, as expected, and that the charge of Si-tag molecules in the detection range (i.e., in the distance of the Debye length from the Si_3N_4 surface) was successfully detected by the SiNW-FET. However, after the Si-tag solution passed the gate insulator, the increased drain current value gradually returned to its baseline level. Assuming that the diffusion of the Si-tags at the interface between the solution containing the Si-tags and the buffer solution is ignored, Si-tags were present on the gate surface for 150 s since the flow rate and the volume of the Si-tag solution were 8 ml/min and 20 ml, respectively. If Si-tags did not bind to the Si_3N_4 surface for this period, the increased drain current would decrease as rapidly as it initially increased. The gradual decrease in I_{DS} suggests that at least some of the Si-tag molecules bound to the Si_3N_4 surface, and that the bound Si-tags gradually dissociated from the surface, probably because of a relatively low affinity for Si_3N_4 . From the result shown in Fig. 5.7, the dissociation rate constant k of Si-tags was calculated, which is given by

$$I_{DS} = (I_{DS,0} - I_{DS,\infty})e^{-k(t-t_0)} + I_{DS,\infty},$$

where t is the measurement time, t_0 is the time at which Si-tags start to dissociate from the Si_3N_4 surface and I_{DS} , $I_{\text{DS},0}$, and $I_{\text{DS},\infty}$ are the drain currents at t , t_0 , and $t = \infty$, respectively. Assuming $t_0 = 200$ s, $I_{\text{DS},0} = 13.1$ nA and $I_{\text{DS},\infty} = 11.3$ nA from Fig. 3.5, a value of $k = 9.0 \times 10^{-3} \text{ s}^{-1}$ was obtained.

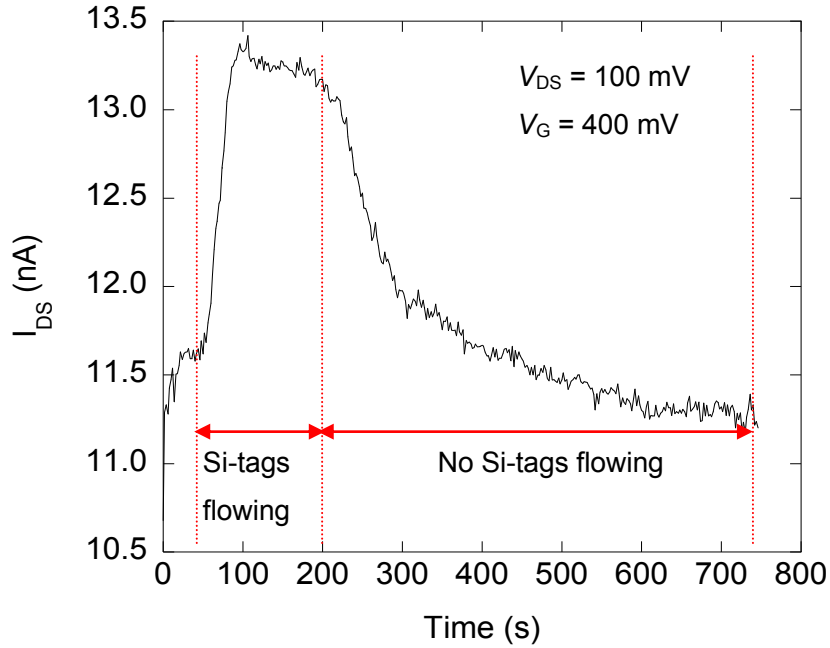


Fig. 5.7. Change over time of drain–source current (I_{DS}) during injection of Si-tag solution into fluidic channel. The drain–source voltage (V_{DS}) and gate voltage (V_{G}) were fixed at 100 and 400 mV, respectively [1].

Immobilizing biomolecules using Si-tags on the gate insulator and detecting the corresponding charge may be possible during the dissociation of Si-tags by improving the measurement method and/or measurement system (e.g., by changing the flow rate and shortening the watercourse).

It is noted that the detection of 5 nM m-antibiotin has been achieved using a biotin-modified SiNW-FET. The sensitivity of our SiNW-FET may increase to an equivalent level by narrowing the width of the SiNW.

5.6. Summary

SiNW-FETs with a very thin Si₃N₄/SiO₂ stack gate insulator on an SOI wafer were fabricated using semiconductor fabrication technology. The threshold voltage of the fabricated SiNW FET changed with the pH of the solution on the gate insulator with a shift of about 60mV/pH, which is consistent with the theoretical value obtained using the Nernst equation. Real-time detection of highly positively charged Si-tag proteins, which bind to SiO₂ surfaces and can be used for immobilization of biomolecules on SiO₂ surfaces were also demonstrated. The fabricated device detected the Si-tag molecules flowing along the channel. However, the results suggest that Si-tags have lower affinity for Si₃N₄.

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Chapter 6 pH sensor and Biosensor Using Single Electron Transistor

Here, as devices using silicon nanoscale structures, pH sensors and biosensors using a silicon single-electron-transistor (Si-SET) are described [1-3].

6.1. Advantage of Biosensor and Ion (pH) Sensor Using Single Electron Transistor

In nanowire FETs, high detection sensitivity is obtained due to the suppression of leakage current in I_d from the percolation paths through the channel even in the dilute range of target molecule concentration [4–6] [Figs. 6.1(a) and 6.1(b)]. Si-SET biosensors have higher sensitivity than nanowire FET ones because of their Coulomb oscillations, as shown in Figs. 6.2(c) and 6.1(d).

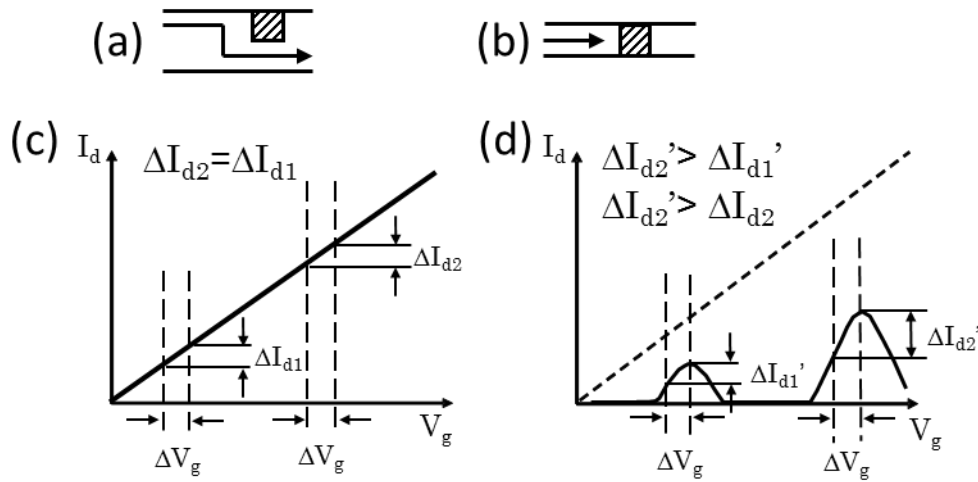


Fig. 6.1. Schematic views to explain the mechanism of high sensitivity in detection of charged species when a nanowire channel FET and a Si-SET are used. (a) When wide channel is used in a FET, a percolation path exists from the source to the drain. Shaded squares represent charged species. Only the small change of drain current (I_d) can be obtained after the charged species bound to the channel. (b) When a nanowire channel is used in a FET, no percolation path forms, leading to the large I_d . Drain current (I_d)–gate voltage (V_g) characteristics are shown for (c) nanowire FET and (d) Si-SET. V_g is change in gate voltage accompanied by binding of biomolecule. In (d), I_d – V_g characteristics of Si-SET (solid line) was obtained by V_g dependence of I_d for nanowire barrier region (broken line) weighted by Coulomb oscillation [3].

Here, I_d is the change in I_d , and V_g is that of V_g accompanied by the binding of biomolecules. The

larger the I_d for a constant V_g , the higher the sensitivity. In nanowire FETs [Fig. 6.1(c)], I_d is almost constant or decreases with increasing V_g for a constant V_d . In Si-SETs [Fig. 6.1(d)], on the other hand, the variation of I_d with V_g for the nanowire barrier region are modulated and weighted by the Coulomb oscillation. This leads to an increase in I_d for a constant V_g at corresponding V_g 's with increasing V_d . Therefore, in principle, the sensitivity in the Si-SET can be higher than that in the nanowire FET.

The I_d - V_g characteristics showed clear Coulomb oscillations for a fabricated Si-SET biosensor in buffer solution at room temperature [Fig. 6.2(a)]. The overall increase in I_d with V_g is due to the effect of I_d - V_g characteristics of the nanowire barrier region. The gate capacitance C_g of an island was estimated from the periodicity of the I_d peaks to be 0.25 aF. The I_d -drain voltage (V_d) characteristics in the inset showed a clear Coulomb blockade region at the V_g of a valley at room temperature.

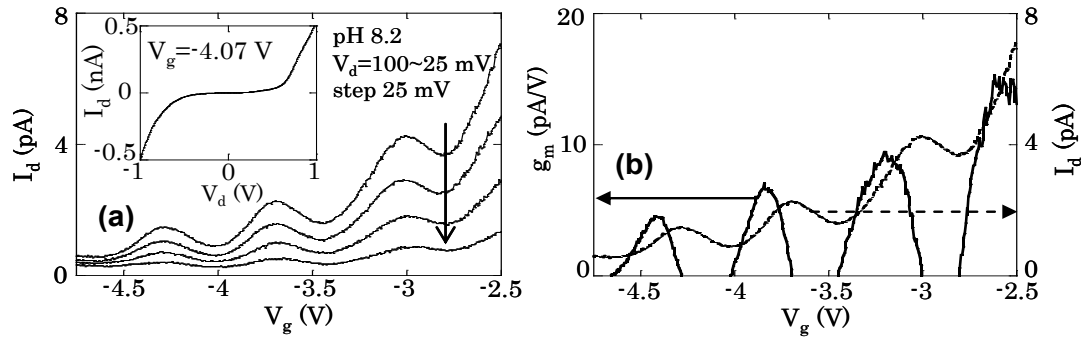


Fig. 6.2. Experimental results of Si-SET biosensor in buffer solution. (a) Drain current (I_d)-gate voltage (V_g) characteristics. V_g was applied using reference electrode. V_d was varied from 100 to 25 mV in steps of 25 mV. Back-gate voltage (V_{bg}) was fixed at 0 V. The inset shows I_d -drain voltage (V_d) characteristics for valley at V_g of -4.07 V. (b) Transconductance (g_m)- V_g characteristics. I_d - V_g curve for $V_d = 100$ mV was used, and only positive g_m values are shown [3].

The junction capacitance C_s ($=C_d$) of the island was estimated from the magnitude of the Coulomb blockade region to be 0.16 aF. As anticipated [Figs. 6.1(c) and 6.1(d)], I_d increased with increasing V_g for a constant V_g , as shown in Fig. 6.2(a), especially at a V_g near the left-side half-maximum of

the I_d peaks. This is also cleared by the increase in g_m with increasing V_g [Fig. 6.2(b)].

The results of theoretical analysis support these findings. The equivalent circuit used for the analysis is shown in the inset of Fig. 6.3(a). The I_d - V_g characteristics for a Si-SET biosensor (solid curve) were obtained using the I_d - V_g characteristics of an FET having only the nanowire barrier region (broken curve) weighted by the analytical formula for Coulomb oscillation [Fig. 6.3(a)]. The used analytical formula for Coulomb oscillation is as follows [7-9]:

$$I_n = \frac{e}{2R_\Sigma C_\Sigma} \frac{(\tilde{V}_{g,n}^2 - \tilde{V}_d^2) \sinh(\tilde{V}_d / \tilde{T})}{\tilde{V}_{g,n} \sinh(\tilde{V}_{g,n} / \tilde{T}) - \tilde{V}_d \sinh(\tilde{V}_d / \tilde{T})},$$

where

$$\tilde{V}_{g,n} = \frac{2C_g V_g}{e} - \frac{(C_g + C_{sub} + C_s - C_d)V_d}{e} - 1 - 2n,$$

$$\tilde{V}_d = \frac{C_\Sigma V_d}{e},$$

$$\tilde{T} = \frac{2k_B T C_\Sigma}{e^2},$$

and

$$R_\Sigma = R_T + R_T,$$

where k_B , e , T , C_g , C_s , C_d , C_{sub} , C_Σ , and n are the Boltzmann constant, elementary charge, temperature, gate capacitance, junction capacitances at source and drain, capacitance between the island and the substrate, total capacitance, and electron number in the island. R_Σ is the resistance of the barrier region, and $R_\Sigma = 2R_T$, where R_T is the resistance of a tunnel junction. T was room temperature; a C_g of 0.25 aF and a $C_s (=C_d)$ of 0.16 aF were used from the results shown in Fig. 3. $C_\Sigma (=C_g+C_{sub}+C_s+C_d)$ was assumed to be 0.6 aF, which is almost the same as that for the Si-SET biosensor for which the results shown in Fig. 3 were obtained. I can see from the calculated results that I_d increases with increasing V_g for a constant V_g at the corresponding V_g 's, especially at a V_g near

the left-side half-maximum of the I_d peaks [Fig. 4(a)]. Indeed, g_m was larger in the Si-SET than in the nanowire FET in the large V_g region [Fig. 6.3(b)]. The I_d reduction due to the effect of correlations in the Si-SET was taken into consideration in the calculation. Namely, an electron must first tunnel off the island before the next one can tunnel on the island in Si-SETs. Therefore, in principle, the sensitivity of a Si-SET can be made much larger than that of a nanowire FET by increasing V_g .

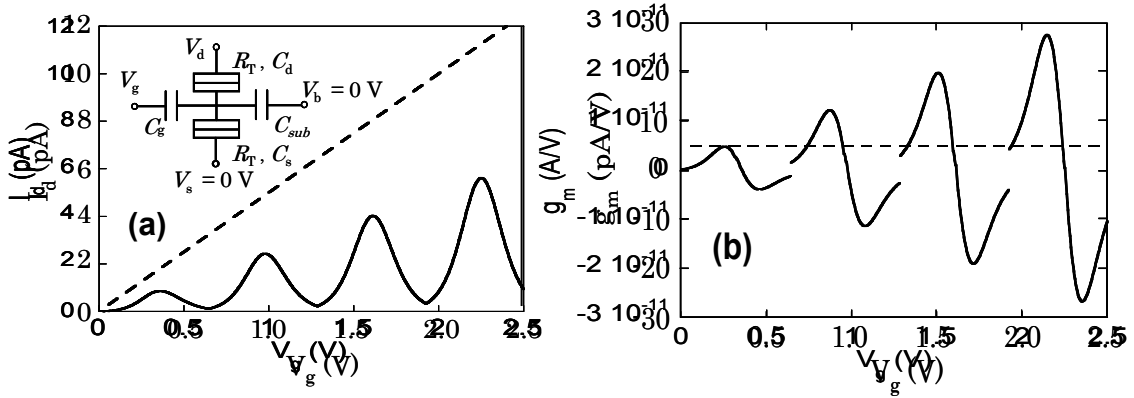


Fig. 6.3. Theoretical analysis. (a) Analytical curves for drain current (I_d)–gate voltage (V_g) characteristics. The inset shows the used equivalent circuit. (b) Transconductance (g_m)– V_g characteristics of a Si-SET. In (b), solid curve was calculated using I_d – V_g characteristics for nanowire barrier region (broken curve) weighted by the formula of Coulomb oscillation in text. In (b), solid curve is for Si-SET, and broken curve is for nanowire barrier region. Discontinuities in g_m appear for Si-SET at V_g 's corresponding to minimum I_d 's between adjacent I_d peaks in (a) due to two different n 's at the V_g [3].

Using a multiple-island channel structure in Si-SETs has two advantages for biomolecular and/or ion sensing. One is high-temperature operation. For ion and/or biomolecule sensing, RT operation is strongly required. To achieve RT operation of a Si-SET with a single island, the island size should be less than 10 nm, which is difficult even with present LSI technologies [10]. A serially connected multiple-island channel structure overcomes this difficulty because the effective total

capacitance of an island decreases, which leads to an increase in the charging energy [10, 11, 12]. The other advantage is that the multiple-island system increases the sensitivity: I_d in the Si-SET easily changes with the dilute target concentration because it changes even if only one target molecule attaches to one of the islands [Fig. 6.4]. Receptor molecules on the island surfaces are attached by surface modifications. If a target molecule happens to meet with one of the receptor molecules, specific binding occurs, and the effective gate voltage in the Si-SET changes, leading to a change in the drain current. The probability of a target molecule meeting a receptor molecule is larger in a multiple island channel structure than in a single-island channel structure.

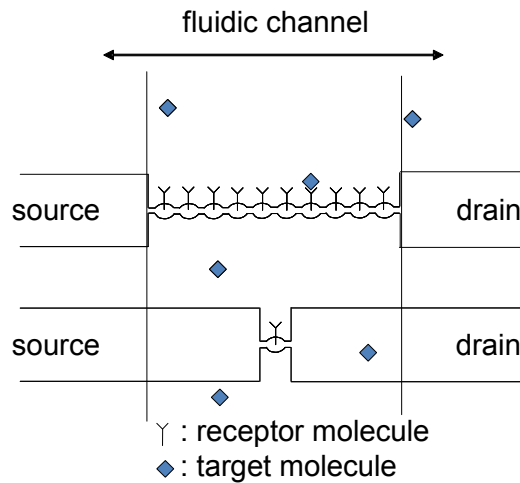


Fig. 6.4. The advantage of long channel [2].

Also, there is an advantage of utilizing Si-SETs to evaluate the target concentration value from only the change in I_d at $V_g = 0$ V. In this case, there is a merit that it is not necessary to sweep V_g for searching a threshold voltage (V_{th}). For that purpose, conventional metal-oxide-semiconductor field-effect transistors with highly doped channel were generally used in accumulation to measure the I_d change at a fixed V_g of 0 V for the pH detection. However, in accumulation highly doped channel shows the metal like conduction: the slope of I_d over V_g is small. Accordingly, it is difficult

for V_{th} change with a small pH change to be detected if relatively large I_d noise exists, leading to the difficulty in high resolution pH detection. Instead, if I use an Si-SET pH sensor with highly doped channel region including Coulomb islands and barriers, high resolution pH detection becomes possible due to the Coulomb oscillation: the slope of I_d over V_g becomes larger. This leads to the merit of high resolution pH detection without sweeping V_g .

6.2. Device Structure and Fabrication Process

Si-SETs with multiple Coulomb islands serially connected in a silicon-on-insulator (SOI) layer. They have 11 islands and a channel length of 3 μm . A p-type (B-doped) SOI (100) wafer (8.5–11.5 $\Omega \cdot cm$) was used. The thicknesses of the top silicon layer and buried oxide on the SOI wafers were 50 and 400 nm, respectively. Two types of devices have been fabricated. One is a Si-SET with the non-doping of the channel for pH sensor, and another is a Si-SET with the doping of the channel for biosensor.

Firstly, the Si-SET with 11 islands for pH sensor have been fabricated. No channel doping was performed. The device fabrication process is as follows. After the etching of the island array with an electron cyclotron resonance etcher using the resist pattern as a mask, subsequent isotropic wet etching in an $NH_4OH/H_2O_2/H_2O$ solution [13] was carried out to reduce the dimensions of the array [Fig. 6.5]. Next, the oxidation was carried out to further reduce the size of the islands and the width of the wire regions, which act as tunnel barriers for electrons. The final island size and wire width was about 50 nm and 30 nm, respectively. The final thickness of the top-Si was about 18 nm. After the source and drain areas were formed by ion implantation of As^+ at 30 keV with a dose of $4 \times 10^{15} cm^{-2}$, Si_3N_4/SiO_2 stacked gate insulators was fabricated as follows. A layer of SiO_2 about 9 nm thick was thermally grown at 850 $^{\circ}C$ in a dry atmosphere followed by the deposition of about 36 nm thick Si_3N_4 by lowpressure chemical vapor deposition at 750 $^{\circ}C$.

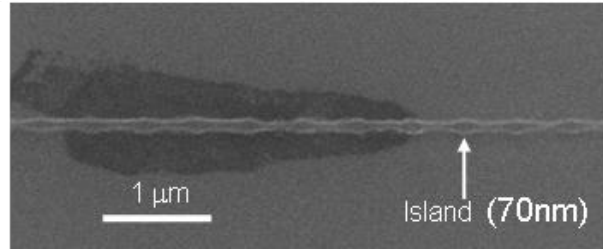


Fig. 6.5. Scanning electron micrograph (SEM) of the channel region of the fabricated Si-SET with 11 islands after dry and wet etching [1].

Secondly, the Si-SET was fabricated for biosensor. Unlike fabrication process of pH sensor, the doping of the top silicon layer was carried out by POCl_3 diffusion at 850°C for 30 min. The doping level was about $3.5 \times 10^{20} \text{ cm}^{-3}$. The fabrication process of a channel region including electron beam lithography and dry/wet etching is similar to that of pH sensor. A scanning electron micrograph of the channel region of a fabricated Si-SET with 11 islands after dry etching is shown in Fig. 6.6. Next, $\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked gate insulators were fabricated. A layer of SiO_2 , about 10 nm thick, was thermally grown at 850°C in a dry atmosphere followed by the deposition of about 90-nm-thick Si_3N_4 by low-pressure chemical vapor deposition at 750°C . The final thickness of the top Si layer was estimated to be about 35 nm (excluding the thickness of the SiO_2). The final width of the nanowire barrier region was about 10 nm and the length was 150–200 nm. The wider region of the island width was about 30 nm and the island length was 50–100 nm. After contact holes and Al electrodes were fabricated, the samples were annealed at 400°C in an H_2 atmosphere.

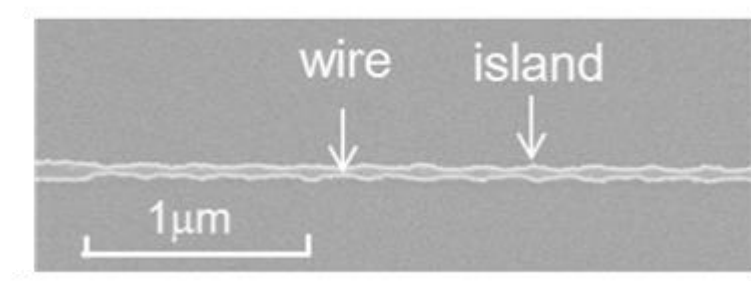


Fig. 6.6. Scanning electron micrograph of fabricated silicon single-electron transistor (Si-SET) with 11 islands after dry etching [2].

6.3. Ion Sensor Using Single Electron Transistor

In this section, Ion sensor using single electron transistor is discussed with measurement results. At first, the Structure and fabrication process for ion sensor is described. Next, the schematic diagram of measurement system for ion sensor is described. Then, the electric characteristics of single electron transistor and pH measurement are discussed.

6.3.1. Measurement System for Ion Sensor

A schematic diagram of our measurement system is shown in Fig. 6.7. A fluidic channel was made of polydimethylsiloxane (PDMS). The volume of the cell was as follows: the size of the fluidic channel on the FET was approximately 3 mm x 1 mm x 100 μm (length x width x height). The entire area of the Si-SET including the Al pad electrodes (0.25 mm²) was 1.2 cm². The joining surface of the PDMS was modified by O₂ plasma treatment and then attached to the Si-SET. An Ag/AgCl reference electrode was used to control the V_g of the Si-SET through a buffer solution. The electrical characteristics were measured using a semiconductor parameter analyzer (B1500A, Agilent).

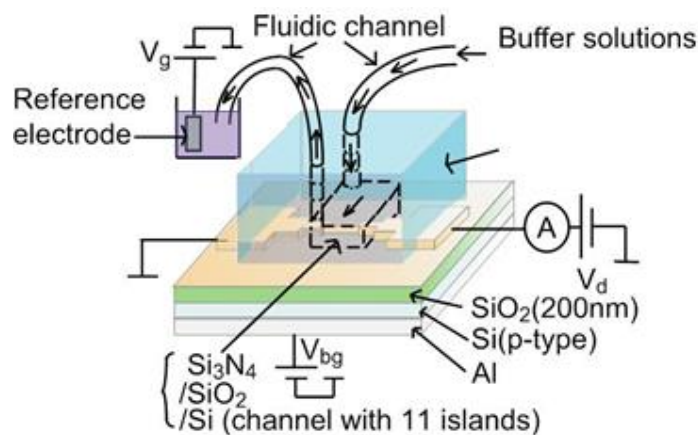


Fig. 6.7 Schematic diagram of measurement system [1].

6.3.2 Electric characteristics of Single Electron Transistor

First, I investigated the electrical characteristics of the fabricated Si-SET under the absence of buffer solutions on the $\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked gate insulators. In this measurement, the gate voltage was applied through the backside of the device (Si substrate of the SOI wafer). Figure 6.8(a) plots I_d versus back-gate voltage (V_{bg}) characteristics at room temperature. The drain-source voltage (V_d) was varied from -1 to 1 mV in V_d steps of 0.2 mV. Two peaks of Coulomb oscillation were confirmed around $V_{bg} = 4$ and 7 V. Figure 6.8(b) shows the contour plot of I_d as a function of V_d and V_{bg} evaluated from Fig. 6.8(a). Clear Coulomb diamonds were observed. The positions of the two peaks of Coulomb oscillation in Fig. 6.5(a) correspond to the constricted parts in Fig. 6.8(b). Therefore, room-temperature Si-SET operation was confirmed for the fabricated devices. The high temperature operation is thought to have been achieved due to a serially connected multiple island system as discussed later.

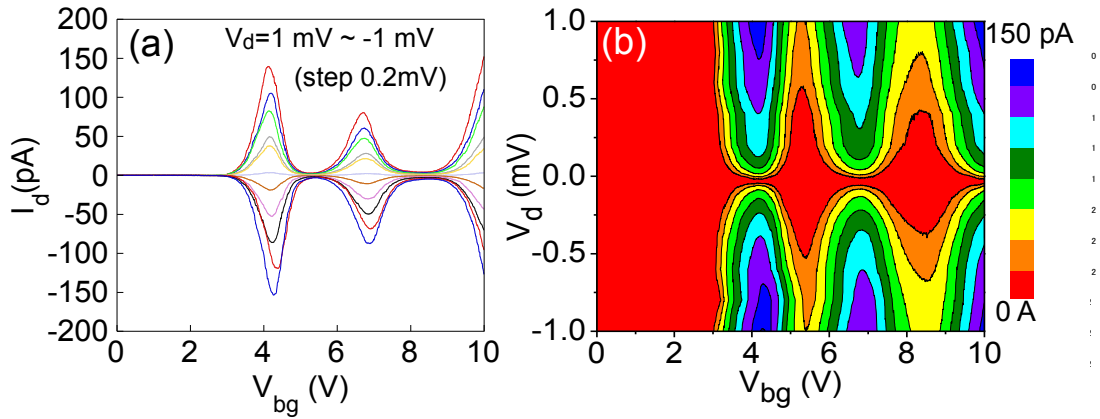


Fig. 6.8. (a) Drain current (I_d) vs back-gate voltage (V_{bg}) characteristics as a function of drain-source voltage (V_d) at room temperature for the fabricated Si-SET with 11 islands. V_d from -1 to 1 mV in V_d steps of 0.2 mV. (b) Contour plot of I_d as a function of V_d and V_{bg} at room temperature. Devices with larger dot size and barrier width did not show Coulomb oscillations [1].

6.3.3 pH Measurement

Figure 6.9 plots the I_d versus V_g characteristics at a V_d of 1 mV for three different buffer

solutions: 50 mM phthalate, pH 4; 50 mM phosphate, pH 7; and 10 mM tetraborate, pH 9. In this measurement, the reference electrode in the buffer solutions was used as a gate while keeping $V_{bg} = 0$ V. I confirmed a linear relationship between the solution potential and V_g ($0 < V_g < 2$ V) with a slope close to one, indicating no electrochemical reactions took place in solution at the V_g range. The flow rate of the solutions was 0.1 μ l /min. The buffer solution was changed from pH 4 \rightarrow 7 \rightarrow 9 \rightarrow 7 \rightarrow 4 to confirm the reproducibility of the pH response. For every pH change, I_d - V_g measurements were carried out three times to investigate the stability under a constant pH. Both in the increase in pH (pH 4 \rightarrow 7 \rightarrow 9) and the decrease in pH (pH 9 \rightarrow 7 \rightarrow 4), the I_d - V_g curves for the same pH coincide well. The small hysteresis (threshold voltage shift less than 5 mV) insures the high resolution pH detection. As can be seen in the figure, a clear Coulomb oscillation peak was observed for each pH value. The peak position varied with the pH of the buffer solution. For $V_g > 2$ V, the measurements were not be carried out due to the large leakage currents between the reference electrode and backgate (typically about 3 nA at $V_g = 2$ V). Because there was no peak in Coulomb oscillation for $V_g < 0$ V in Fig. 6.8, this peak is assumed to correspond to the first peak of Coulomb oscillation (around 4 V of V_{bg}) in Fig. 6.8(a).

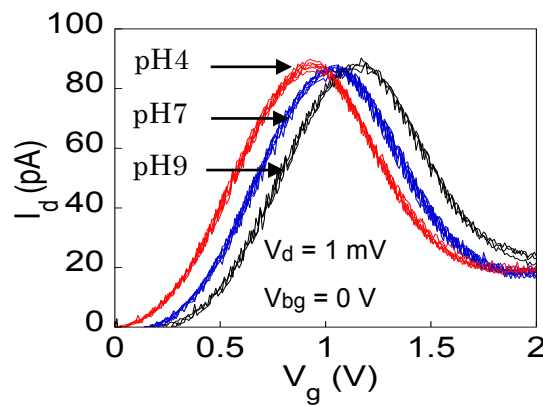


Fig. 6.9 Drain current (I_d) vs gate voltage (V_g) characteristics of the Si-SET with 11 islands for three different pH values at room temperature. The drain-source voltage (V_d) was fixed at 1 mV. The back-gate voltage (V_{bg}) was also fixed at 0 V. The leakage current between the reference electrode and source/drain contact is very small and keeping the value within 2 pA less than the noise level at the V_g range from 0 to 2 V, ensuring the measurement reliability [1].

A summary of the pH response characteristics of the Si-SET is plotted in Fig. 6.10. Because there is some noise in the measured I_d - V_g curves in Fig. 6.6, each measured I_d - V_g curve of Coulomb oscillation was fitted using a least-squares program, and the V_g values were obtained at the left side half maximum current of each fitted curve in order to precisely evaluate the pH sensitivity. The obtained V_g value (V_g half) was shifted in the positive (negative) direction as the pH of the buffer solution was increased (decreased). The slope of the calibration curve (V_g half versus pH curve) is about 44 mV/ pH , which agrees well with previous experimental results (46–56 mV/ pH) [14]. The slight difference in our experimentally obtained value and the theoretical value (58 mV/ pH , 20 °C) may be due to the oxygen content in the Si_3N_4 layer. These results show that reproducible pH responses were obtained with the fabricated Si-SET.

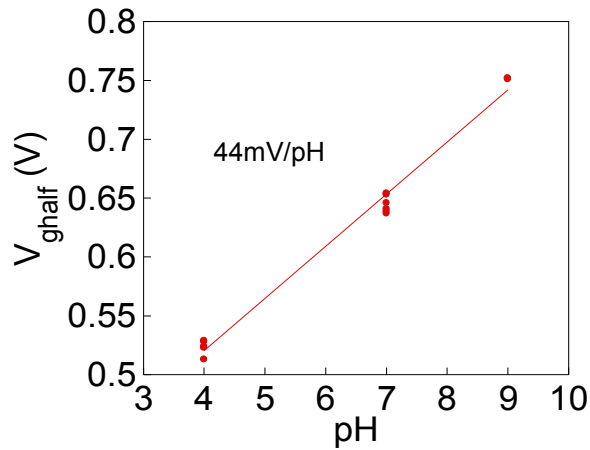


Fig. 6.10. pH response characteristics of the fabricated Si-SET with 11 islands at room temperature [1].

For ion and/or biomolecule sensing, room-temperature operation is strongly required. To achieve room-temperature operation of an Si-SET with a single island, the island, and junction sizes should be reduced to less than 10 nm in order to reduce the total capacitance [10]. However, it is difficult to fabricate such structures reproducibly by using currently available LSI fabrication

techniques. One way to overcome the difficulty is to utilize serially connected islands instead of a single island. In such a multiple-island system, the effective total capacitance of each island decreases compared with that in a single-island system because the junction capacitances are connected in series [10, 12]. This leads to an increase in the charging energy of each island and to an increase in the operation temperature. In other words, to enable room-temperature operation, a multiple-island system can use a larger island than that used by a single-island system. Moreover, Si-SETs with serially connected islands can suppress cotunneling [15], which increases the valley current of Coulomb oscillation and prevents higher temperature operation [16]. To date, an Si-SET with multiple islands connected in series to an exclusive-OR (XOR) circuit, which achieved room-temperature operation have been applied [11]. Therefore, I used the multiple-island system to realize room-temperature operation of an Si-SET for highly sensitive *pH* sensing in this study. In fact, Coulomb oscillations were not obtained at room-temperature in Si-SETs with a single-island system in this study.

6.4. Biosensor Using Single Electron Transistor

In this section, biosensor using single electron transistor is discussed with measurement results. At first, the Structure and fabrication process for biosensor is described. Next, the schematic diagram of measurement system for ion sensor is described. Then, the Si_3N_4 gate insulator surface chemical modification for biotin-streptavidin binding and prostate specific antigen (PSA) detection is explained. Finally, the streptavidin and PSA detection are discussed.

6.4.1. Measurement System

A schematic diagram of our measurement system is shown in Fig. 6.11 by using biotin-streptavidin binding. A solution chamber was attached to the $\text{Si}_3\text{N}_4/\text{SiO}_2$ gate insulator. The

channel region including all barriers and islands in the Si-SET was inside the solution chamber region. The diameter of the chamber was 0.5 cm. An Au reference electrode was used to control the gate voltage (V_g) of the Si-SET through a buffer solution. The electrical characteristics were measured using a semiconductor parameter analyzer (B1500A, Agilent).

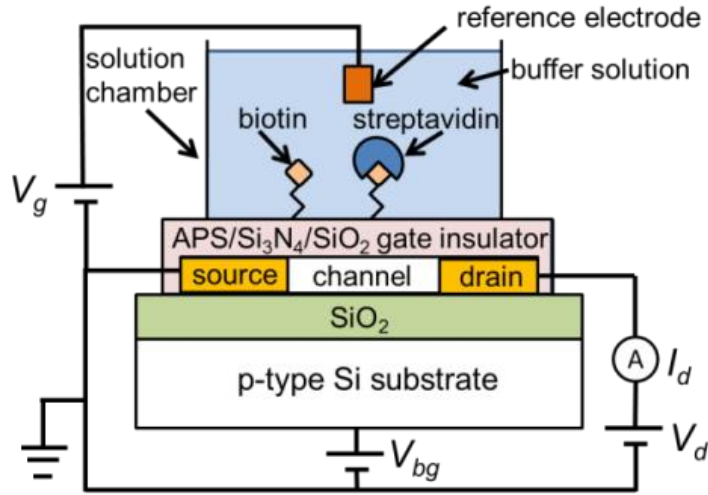


Fig 6.11. Schematic diagram of measurement system [2].

6.4.2 Si₃N₄ Gate Insulator Surface Chemical Modification

The Si₃N₄ gate insulator surface chemical modification sequence is shown in Fig 6.12 for specific binding of biotin-streptavidin. The Si₃N₄/SiO₂ gate insulator surface was chemically modified. To remove organic contamination, the surface of the Si₃N₄ layer was cleaned in a solution of H₂O/H₂O₂/NH₄OH (weight ratio of 18:1:1) at 80 °C for 10min [17]. After being rinsed with pure water, the surface was cleaned again with 1M NaOH for 1h at RT [18]. To silanize the Si₃N₄ surface [i.e., to form an aminopropylsiloxane (APS) surface], the surface was soaked in 2 wt.% 3-aminopropyltriethoxysilane (APTES) in anhydrous toluene [18] at 60 °C for 10 min [Fig. 6.12(a)]. It was then rinsed in anhydrous toluene and dried immediately in vacuum at 110 °C for 1h [18]. After silanization, biotin (250 µg/ml) was reacted with the APS-terminated Si₃N₄ surface at RT for

30min to obtain a biotinylated surface as shown in Fig.6.12(b). Finally, the biotinylated surface was reacted with 10 $\mu\text{g/ml}$ streptavidin for 30 min as shown in Fig. 6.12(c) and (d).

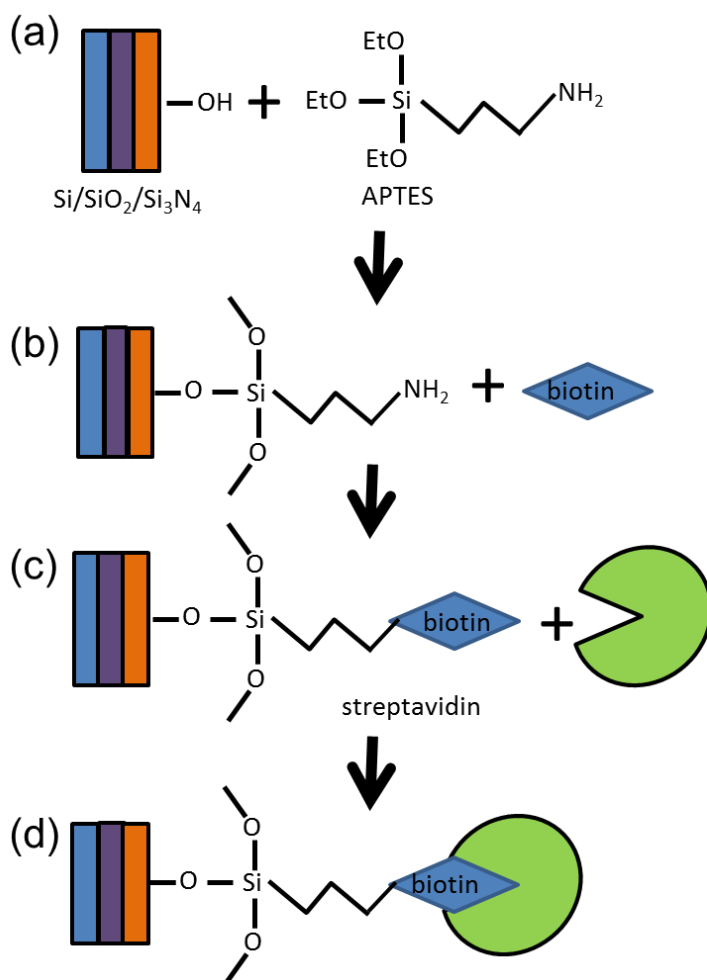


Fig. 6.12. The Si_3N_4 gate insulator surface chemical modification sequence for streptavidin detection.
 (a) Forming of APS surface. (b) Biotin binding to APS surface. (c) Biotin-Streptavidin specific binding (d) Detection of streptavidin

On the other hand, the chemical modification of the gate insulator surface for the anti-PSA reacted one is shown in Fig. 6.13. To remove organic contamination, the surface of the Si_3N_4 layer was cleaned in a solution of $\text{H}_2\text{O}/\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$. After being rinsed with deionized water, the surface was cleaned again with 1M NaOH for 1 h at RT. To form an APS surface, the surface was soaked in

10 wt.% APTES in anhydrous toluene at RT for 30 min [Fig. 6. 13(a)]. The amino-silanized Si_3N_4 surface was then rinsed in deionized water and dried immediately in vacuum at 110 °C for 30 min. Next, the amino-silanized Si_3N_4 surface is soaked in a mixed solution (volume ratio of 1:1) of a 25 wt.% glutaric dialdehyde solution with 0.01 g of NaBH_3CN per 1ml and 250 mM phosphate buffer solution for 4 h at room temperature as shown in Fig. 6.13(b). Then, the aldehyde-functionalized Si_3N_4 surface is coupled to anti-PSA by reaction of 125 $\mu\text{g}/\text{ml}$ anti-PSA in pH 8.4 phosphate buffer solution containing 4 mM NaBH_3CN for 4 h at RT as shown in Fig. 6.13(c). Finally, the unreacted Si_3N_4 surface aldehyde is blocked by using 50 mM ethanolamine containing 4 mM NaBH_3CN for 10 min. After that the detection of PSA was carried out by PSA and anti-PSA binding [Fig. 6.13(d) and 6.13(e)].

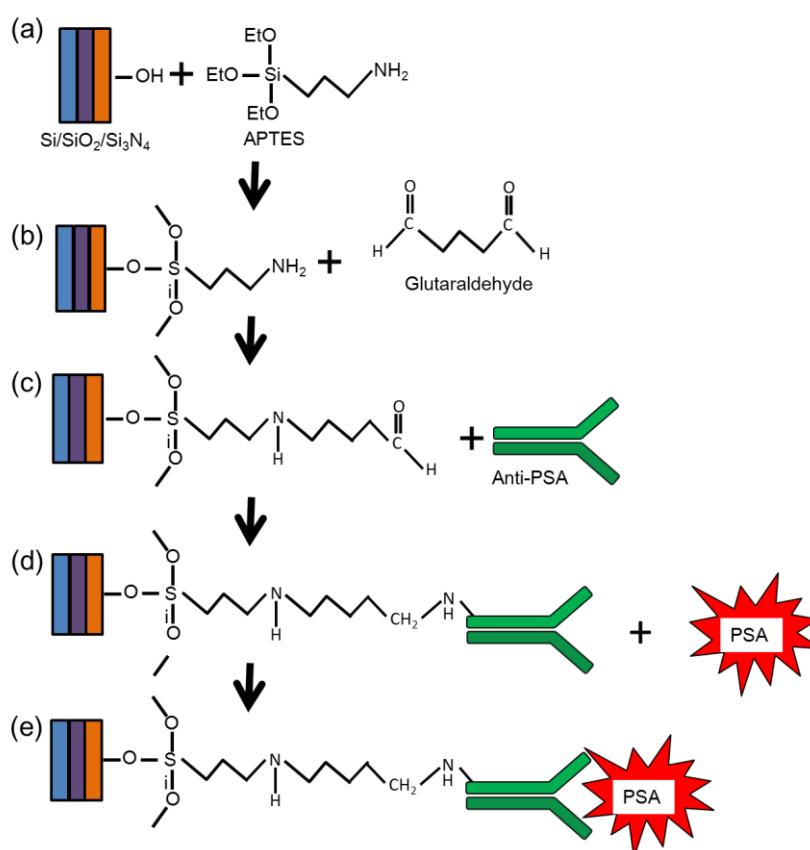


Fig. 6.13. The Si_3N_4 gate insulator surface chemical modification sequence for PSA detection. (a) Forming of APS surface. (b) Forming of aldehyde on APS surface. (c) Anti-PSA binding to aldehyde. (d) Anti-PSA and PSA binding. (e) Detection of PSA.

6.4.3 Streptavidin Detection

Figure 6.14 shows the results of biomolecule detection using the well-known ligand-receptor binding of biotin-streptavidin. To avoid the problem of Debye screening, I chose the ion concentrations in the buffer solution such that the Debye screening length was sufficiently long to enable detection and sufficiently short to screen unbound biomolecules [19]. At the same time, the pH of the buffer solutions was set to 8.0–8.2 since the isoelectric point of streptavidin is pH 5–6 [20]. Therefore, the streptavidin was negatively charged in the buffer solution. The drain current (I_d)-gate voltage (V_g) characteristics were measured before and after the biotinylation of the APS-terminated surface and after the subsequent addition of 10 $\mu\text{g/ml}$ streptavidin to the biotinylated surface. For each surface modification, the electrical characteristics were obtained five times to confirm reproducibility. As can be seen in Fig. 6.14(a), the I_d - V_g curve differed for each surface modification. For the reason described later, I evaluated the V_g shift in each curve on the left side of the peak. At the half-maximum peak current, the V_g value (V_g half) shifted -220mV due to the attachment of biotin to the APS-terminated surface, which is consistent with the positive charge of biotin [Fig. 6.14(b)]. In contrast, the successive addition of 10 $\mu\text{g/ml}$ streptavidin resulted in an increase in V_g half (the V_g shift = +150 mV), which is consistent with the negative charge of streptavidin. If I fixed the V_g (= 5.95 V) at V_g half for APS-terminated surface, I can observe correspondingly that I_d increases (the average I_d shift = +350 pA) after the attachment of biotin and then decreases (the average I_d shift = -220 pA) after the successive binding of streptavidin. These experimental results demonstrate the achievement of biomolecule detection based on a Si-SET using the binding of biotin-streptavidin.

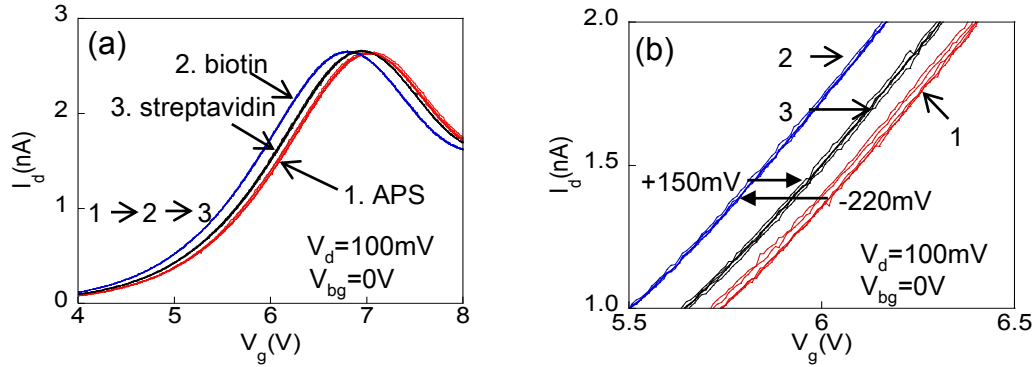


Fig. 6.14. Drain current (I_d) vs. gate voltage (V_g) characteristics of Si-SET with multiple islands for biotin-streptavidin binding at room temperature. Drain-source voltage (V_d) was fixed at 100 mV. Back-gate voltage (V_{bg}) was fixed at 0V. The results were for 10 μ g/ml streptavidin. (b) Curves in V_g region from 5.5 to 6.5V for (a) [2].

The detection of streptavidin was carried out at the dilute concentration of 1 ng/ml (16 pM) by using other Si-SET as shown in Fig. 6.15. The addition of streptavidin to the biotinylated surface resulted in an increase in threshold voltage (V_{th}), namely, a positive ΔV_g . This is consistent with the streptavidin's negative charge in solution at pH 8.1. The ΔV_g was 90 mV.

In the recent reports as to streptavidin detection of the SiNW-FET fabricated by top-down processes, the detection of streptavidin with 10 fM ($= 0.53$ pg/ml) was reported by Stern et al [21]. Compared with the 0.53 pg/ml, the value of 1 ng/ml is larger. It should be noted that the detection measurement at the smaller concentration than 1 ng/ml has not been tried in my biosensor. Therefore, the detection in a 0.1 pg/ml order should be performed in future. In addition, one of the method to increase ΔV_g is to increase pH of buffer solution, which leads to increase the effective charge of streptavidin/

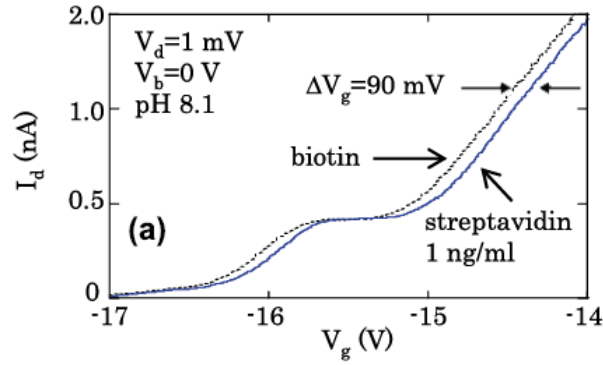


Fig. 6.15. Drain current (I_d) vs. gate voltage (V_g) characteristics of Si-SET with multiple islands for biotin-streptavidin binding at room temperature. Streptavidin concentration of 1 ng/ml [3].

6.4.4 Prostate Specific Antigen (PSA) Detection

Immunodetection of PSA using a Si-SET biosensor was achieved, as shown in Fig. 6.16. The PSA detection level was 4 ng/ml, which is the required detection level for practical use. Due to the isoelectric point (6.9) of PSA, the binding event of PSA to the anti-PSA reacted surface in solution at pH 7.5 is equivalent to the binding of a negative charge. This should result in a positive ΔV_g , which is consistent with the results shown in Fig. 6.16. The ΔV_g was 30 mV.

Kim et al. reported the PSA detection of 1 fg/ml [22]. However, the measurement was performed under the flow of the SPA solution: The conductance was decreased by the anti-PSA and PSA binding during the PSA solution flowing and then restored to the initial levels on the injection of buffer solution which does not include PSA. The restoration is due to the dissociation of anti-PSA and PSA binding. In contrast, the ΔV_g was 30 mV due to the anti-PSA and PSA binding was obtained clearly after the buffer solution which does not include PSA in Fig. 6.16. Therefore, the fabricated biosensor is considered to be more reliable than that of Kim et al.

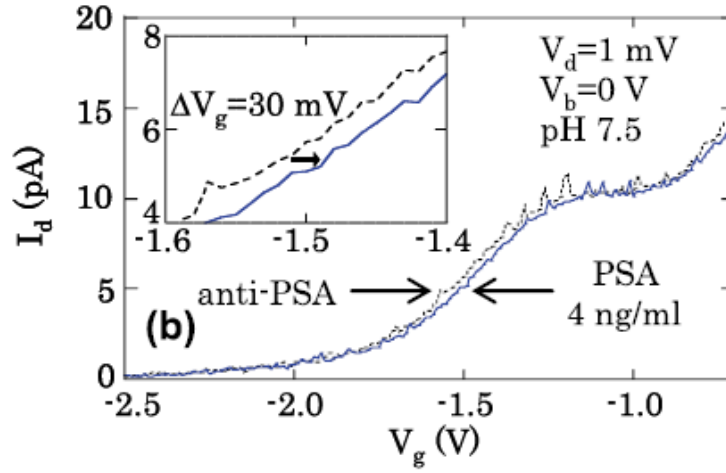


Fig. 6.16. Drain current (I_d)–gate voltage (V_g) characteristics of Si-SET biosensor. PSA concentration of 4 ng/ml. The inset shows curves in V_g region from -1.6 to -1.4 V. Problem of Debye screening was avoided by setting ion concentrations in buffer solutions such that Debye screening length [3].

6.5. Summary

In summary, a Si-SET was fabricated for pH and biosensors integrated on a single chip. The channel structure with serially connected islands can operate at room temperature and has higher sensitivity. Clear Coulomb oscillations and Coulomb diamonds were confirmed at room temperature.

First, clear pH responses of I_d - V_g characteristics were obtained by using Coulomb oscillations despite the existence of I_d noise. The slope of the calibration curve was 44 mV/ pH , which agrees well with previous experimental results (46–56 mV/ pH).

Second, biomolecule detection was achieved using a Si-SET for highly sensitive detection. After chemical modification of the Si_3N_4/SiO_2 gate insulator surface with 3-aminopropyltriethoxysilane and biotin, streptavidin of 1 ng/ml was detected on the basis of a clear shift in the gate voltage at the Coulomb oscillation.

Third, the PSA of 4 ng/ml was detected by utilizing anti-PSA and PSA binding, which is

the required detection level for practical use.

Coulomb oscillation has a possibility to increase the transconductance (g_m), and a larger g_m leads to higher sensitivity to a charged target. Since a Si structure enables label-free biomolecule and/or ion sensors to be integrated into an LSI chip, a Si-SET with multiple islands should enable the integration of a sensor system on a single chip for multiplexed detections and simultaneous diagnoses.

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Chapter 7 Conclusion

7.1 Conclusion

Silicon nanoscale structures having potential to be utilized for realizing various functional devices have been fabricated and applied to the functional devices such as a functional gate metal-oxide-semiconductor field effect transistor (MOSFET), a silicon nanowire FET (SiNW-FET) with a thin gate insulator, and a silicon single-electron-transistor (Si-SET). Here, one-dimensional nanoscale structure as to the tunnel gate oxide thickness and two-dimensional nanoscale structures as to the charge trap layer area were used in the functional gate MOSFET. On the other hand, the SiNW-FET with a thin gate oxide structure used two types of nanoscale structure. One type is a two-dimensional nanoscale structure as to the width/thickness of the nanowire and the other is a one-dimensional nanoscale structure as to the gate insulator thickness.

Functional gate MOSFETs using tunnel injection and ejection of trap charges enabling self-adjustable threshold voltage (V_{th}) as the devices of CMOS logic application were fabricated for ultralow power operation. The V_{th} shifted negative direction after the positive gate voltage (V_g) was applied to gate electrode, which shows that the trapped electrons were indeed ejected from the charge trap layer to the gate electrode. By the application of negative V_g , V_{th} returned to the voltage close to the initial V_{th} . This self-adjustment leads to the increase in on-current without increasing off-current. The device reliability, including endurance characteristics for electron ejection/injection and the degradation mechanism of tunnel gate oxide were investigated. By reducing the area of charge trap layer and tunnel oxide thickness in device, the CMOS logic operation is considered to be realized with low power operation.

SiNW-FET with an extremely thinner and more reliable Si_3N_4 gate insulator (42 nm Si_3N_4 /10 nm SiO_2 for ion detection and 19 nm Si_3N_4 /8 nm SiO_2 for Si-tag detection) compared with

these of the previous works (approximately Si_3N_4 100nm/ 100nm SiO_2) were fabricated for highly sensitive ion and biomolecule detection. The influence of target's charge on the channel of SiNW-FET becomes larger because of the decrease in length between the target and channel. The thin gate insulators enable to increase sensor sensitivity without increasing leakage current through the gate insulator.

Fabricated SiNW-FETs acted as hydrogen sensor (*pH* sensor) in the buffer solution, which detected the charge of hydrogen bound on the Si_3N_4 gate insulator surface of the channel. When *pH* of buffer solution was changed, the *pH* sensor showed different drain current (I_d)- V_g characteristics, which indicates that the fabricated *pH* sensor can respond to the change of hydrogen concentration properly. Also, the fabricated SiNW-FET detected biomolecule's charges flowing on the gate insulator surface. The chemical modification of gate insulator surface to bind target was established.

Highly sensitive ion sensor and biosensor utilizing silicon single-electron-transistor (Si-SET) were fabricated. Fabricated Si-SET with multiple islands showed clear Coulomb oscillation at room temperature by reducing effective capacitance of islands. The Si-SET sensor clearly detected *pH* of buffer solution using Coulomb oscillation. The detection of streptavidin of 1 ng/ml was realized utilizing specific binding between biotin and streptavidin. When streptavidin bound biotin on Si_3N_4 gate insulator of Si-SET, the peak position of Coulomb oscillation of Si-SET shifted with gate voltage. PSA with 4 ng/ml was detected utilizing anti-PSA and PSA binding, which is the required detection level for practical use. Transconductance of I_d - V_g characteristics increases due to the Coulomb oscillation, which leads to highly sensitive detection of ions and biomolecules.

Therefore, silicon nanoscale structures having potential to be utilized for realizing various functional devices have been fabricated and several functional devices has been realized using the structures. All dimensions of nanostructure (from one dimension to three-dimension) were investigated: The fabricated devices cover all dimensions of nanostructure.

7.2 Academic Impact

1. The fabrication method was established for SiNW-FET biosensor with a thin Si₃N₄ gate insulator to realize highly sensitive ion/biomolecule detection.
2. Ion sensor and biosensors utilizing Si-SETs were proposed and fabricated for highly sensitive detection, demonstrating the feasibility for practical use.
3. Functional gate MOSFETs were fabricated for low power operation of CMOS logic application. By reducing the area of charge trap layer, the possibility of increasing the device reliability was demonstrated.

7.3 Industrial Impact

1. The detections of hydrogen ion, streptavidin, PSA utilizing Si-SET were realized for the first time for highly sensitive ion/biomolecule detection.
2. The breakdown mechanism of the gate insulator was clarified for the functional gate MOSFET for CMOS logic operating with low power.

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Appendix A. Process sheet of the functional gate MOSFET

インジケータ		使用装置		処理条件		ウェット					ウェット					ウェット					ウェット					ウェット																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																															
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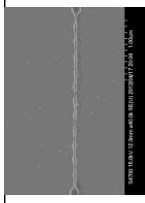

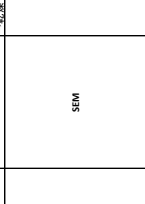
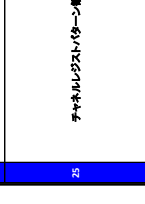
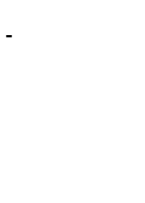
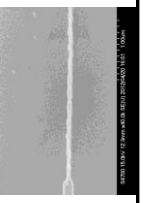
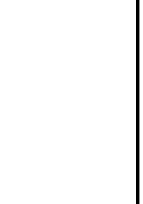
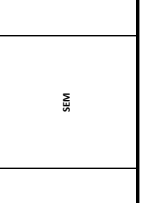


10	ソース/ドレイン形成	A1 塗入/イオン注入装置	A1 300W / 1.5 kV 500 mA 100 W P25 (CAN10%) / H2O2 (10%) / 500:1:157 (ml) 10min → 乾燥 → 水洗 5min 3min	0	0	0	0	0	0
		S1 洗浄/SH de et	水洗 30min → 乾燥 → 水洗 5sec → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		RCA 洗浄/UVC/UV 露光ソフト	水洗 30min → 乾燥 → 水洗 5sec → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A2 塗布/UV 露光ソフト	P25 (CAN10%) / H2O2 (10%) / 500:1:157 (ml) 10min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
11	膜厚調整/露光	A2 塗布/UV 露光ソフト	P25 (CAN10%) / H2O2 (10%) / 500:1:157 (ml) 10min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		露光/露光ソフト	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		露光/露光ソフト	BHF/H2O+1:1 30sec → 水洗 8min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		露光/露光ソフト	P25 (CAN10%) / H2O2 (10%) / 500:1:157 (ml) 10min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
12	コンタクトホール形成	コンタクトホールマスク用レジスト塗布/スピニング	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		コンタクトホールマスク用レジスト塗布/スピニング	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		コンタクトホールマスク用レジスト塗布/スピニング	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		コンタクトホールマスク用レジスト塗布/スピニング	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
13	A1 電線形成	A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
14	A1 電線形成	A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0
		A1 電線形成	180°C 3min → HMDS 塗布 レジレ1 → 180°C 2min → 水洗 1min → 乾燥 → 水洗 5min 3min → 乾燥	0	0	0	0	0	0

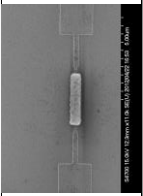
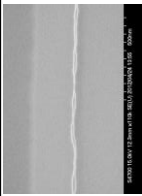
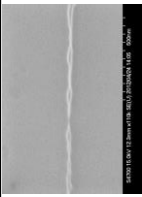
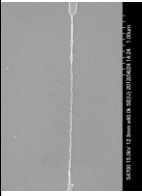
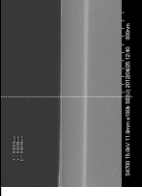
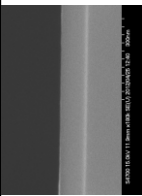

Appendix B. Process sheet of the SiNW-FET

ナノワイヤトランジスタ作製工程表				
大工程名		詳細工程名	使用装置	詳細条件など
ロット投入				
ロット投入	1	ロット投入		本ロット5枚、予備?枚、モニタ用?枚 計?枚 p-Si 8-12Ω cm (100)ジャスト
マーク形成				
マーク酸化	2	SC-1洗浄, HF処理		DIR 5+3分 → SC-1 80℃ 10分 → DIR 5+3分 → 0.5%HF 1分 → DIR 5+3分 → SD 4分 *SC-1溶液(NH4OH:H2O2:H2O=36:720:1680)
	3	酸化	poly-酸化炉	74nm, 1000℃ 100分, O2=2 l/min
	4	膜厚測定	Nanospec	
	5	HMDs塗布		塗布前ベーク180℃3分 → HMDs塗布 → ベーク180℃2分
マーク リングラフィ	6	レジスト塗布		ポジ型レジスト ZEP520A塗布 (レシピ4) → ベーク180℃ 10分
	7	露光	HL700 EB	ドーズ 90μ C/cm2 ジョブ名: KUDO_WAFERB_0710 KUDO_CHIPB_0710 KUDO_CHIPN_0710
	8	現像		キシレン浸漬 6分→IPAリンス20秒→ 超純水洗浄1分→SD4分
	9	ポストベーク		130℃ 3分 (エッチング直前に実行)
マーク エッチング	10	SiO2 エッチング	SiO2 RIE	CF4/H2= 20/7sccm Vdc -410V RF 159/1W 30mTorr 2分30sec
	11	Si エッチング	SiO2 RIE	CF4= 20sccm Vdc -410V RF 159/1W 25mTorr 2分
	12	SiO2 エッチング	SiO2 RIE	CF4/H2= 20/7sccm Vdc -410V RF 159/1W 30mTorr 15min
	13	Si エッチング	Si ECR	Cl2=40sccm Vdc -80V 3min
	14	アッシング	Asher	O2 = 50sccm 0.6Torr 200W 10分
	15	酸化膜除去		63BHFU(ダイキン, 界面活性剤入) 5分 DIR 5+3分 SD 8分
	16	SH洗浄		SH(H2SO4:H2O2=500:167) 10分 → DIR 5+3分 → SD4分
アクティブ領域形成				
アクティブ領域 形成リングラフィ	15	HMDs塗布		塗布前ベーク180℃3分 → HMDs塗布 → ベーク180℃2分
	16	レジスト塗布		ネガ型レジスト SAL601 SR2 塗布 (レシピ6) → ベーク 105℃ 1分
	17	露光	HL700 EB	ドーズ 36 μ C/cm2 ジョブ名: KUDO_BIO_0710 レベル1 KUDO_NOMAL_0710 レベル1
	18	PEB(Post Exposure Bake)		105℃ 1分
	19	現像		MF-CD26 6分 超純水洗浄1分 SD4分
	20	SEM観察		
アクティブ領域 形成エッチング	21	SOI エッチング	Si ECR	Cl2=40sccm Vdc -80V 26sec~50sec
	22	アッシング	Asher	O2 = 50sccm 0.6Torr 200W 10分
	23	SH洗浄		SH(H2SO4:H2O2=500:167) 10分 → DIR 5+3分 → SD4分
S/D形成				
インプラマスク用 HTO成膜	24	モニタウェハ追加		追加せず
	25	SC-1, HF洗浄		DIR 5+3分 → SC-1 80℃ 10分 → DIR 5+3分 → 0.5%HF 1分 → DIR 5+3分 → SD 4分 ※SC-1溶液(NH4OH:H2O2:H2O=36:720:1680)
	26	HTO成膜	SiO2 LPCVD	SiH4:N2O=40:200sccm 0.258Torr 15min
	27	膜厚測定	Nanospec	
インプラ用 マスクリングラ フィ	28	HMDs塗布		塗布前ベーク180℃3分 → HMDs塗布 → ベーク180℃2分
	29	レジスト塗布		ポジ型レジスト ZEP520A塗布 (レシピ4) → ベーク180℃ 10分
	30	露光	HL700 EB	ドーズ 90μ C/cm2 ジョブ名: KUDO_INPLAB1_0710 KUDO_INPLAB2_0710
	31	現像		キシレン浸漬 6分 IPAリンス 20秒 DIR1分 SD4分
	32	ポストベーク		130℃ 3分
n+ インプラ	33	イオン注入	イオン注入装置	イオン: As エネルギー-20 keV ドーズ 5e14 cm-2 使用ホルダ2inc 7° off
	34	アッシング	Asher	O2=50sccm 0.6Torr 10分
	35	SH洗浄		SH(H2SO4:H2O2=500:167) 10分 → DIR 5+3分 → SD4分
インプラアニール	37	SC-1, HF洗浄		DIR 5+3分 → SC-1 80℃ 10分 → DIR 5+3分 → SD 4分 ※SC-1溶液(NH4OH:H2O2:H2O=36:720:1680) ※HFは未処理
	38	インプラアニール	poly-Si 酸化炉	850℃ N2:8slmで2minでロード → N2:8slmで5minプレヒート → N2:3slmで15min → N2:8slmで2minでアンロード

ゲート形成			
ゲート酸化	39	モニタウェハ追加	3枚追加(ペアのシリコンウェハ)
	40	SC-1, HF洗浄	DIR 5+3分 → SC-1 80℃ 10分 → DIR 5+3分 → 0.5%HF 1分くらい 裏面と膜厚測定部分が撥水することを確認する → DIR 5+3分 → SD 4分 SC1溶液(NH4OH:H2O2:H2O=36:720:1680)
	41	ゲート酸化	poly-Si 酸化炉 膜厚10nm、1000℃ 4分、O2=2 (l/min)
	42	膜厚測定	分光エリブソ ペアシリコン1枚を使って測定
SiN 堆積	43	Si3N4 堆積	SiN LPCVD 750℃ SiH2Cl2:10sccm NH3=100sccm 0.120Torr 26min ペアで条件だし
	44	膜厚測定	分光エリブソ 膜厚参照部分で測定(Fitはおそらく悪い)
コンタクトホール 形成リソグラフィ	45	HMDS塗布	塗布前ベーク180℃3分 → HMDS塗布 → ベーク180℃2分
	46	レジスト塗布	ポジ型レジスト ZEP520A塗布 (レシビ4) → ベーク180℃ 10分
	47	露光	HL700 EB ドーズ 90μ C/cm2 ジョブ名: KUDO_BIO_0710.2 KUDO_NOMAL_0710.1
	48	現像	キシレン浸漬 6分 IPAリンス 20秒 DIR1分 SD4分
コンタクトホール 形成エッチング	49	ポストベーク	130℃ 3分
	50	Si3N4エッチング	CDE 50sec CF4=70,O2=100, N2=17sccm 0.8Torr, micro波1kW ペアで条件だし
	51	SiO2 エッチング	BHF 10sec → DIR 5+3分 → SD4分
	52	膜圧測定	膜厚参照部分で測定 (Fitはおそらく悪い MSEの値が多分20近くになる)
AI電極形成	53	SH洗浄	SH(H2SO4:H2O2=500:167) 10分 → DIR 5+3分 → SD4分
	54	モニタウェハ追加	2枚
	55	HF処理	HF=2.5, H2O2=10, H2O=487.5 2分 水洗2分 乾燥2分
	56	アルミ蒸着	表面500nm 裏面500nm
アルミ電極 形成リソ	57	HMDS塗布(必ず裏面が最初)	塗布前ベーク180℃3分 → HMDS塗布 → ベーク180℃2分
	58	レジスト塗布	IP3300 塗布 (レシビ10) → ベーク 90℃ 3分
	59	HMDS塗布(表面処理)	塗布前ベーク180℃3分 → HMDS塗布 → ベーク180℃2分
	60	レジスト塗布	ネガ型レジスト SAL601 SR7 塗布 (レシビ6) → ベーク 105℃ 1分
	59	露光	HL700 EB ドーズ 30 μ C/cm2 ジョブ名: KUDO_BIO_0710.3 JOBのつくり間違いが怖いので、モニタウェハ使って確認 ジョブ名はKUDO_HAISENB_0710.1
	60	PEB(Post Exposure Bake)	105℃ 5分
	61	現像	DEVELOPER CONCENTRATE 10分 → 超純水洗浄1分 SD4分
	62	ポストベーク	110℃ 2分 (エッチング直前に実行)
アルミ電極 エッチング	63	Al ウェットエッチング	H3PO4:H2O:HN03:CH3COOH=500:34:34:100m 10min → DIR 5+3分 → SD4分
活性化アニール	64	剥離洗浄	剥離液 80℃ 10分 IPAリンス7分 水洗5+3分 乾燥4分
	65	Post Metallization Anneal	PMA炉 400℃ H2=0.5L/min, N2 2L/min 30分

Appendix C. Process sheet of the Si-SET

15	SH洗浄	SHドラフト	H2SO4(99%)H2O2(10%)=500:167(ml) 10min →水洗5min3min →クリーンROXに回収	0	0	0	0	0	
16	RC洗浄	UPCの膜ドラフト	→80℃ H2O2/H2O2(10%)NH3(128%)=1680:720:36 (ml) 10min →水洗5min3min →HF(50%)H2O=100:1900 (ml) 5min →水洗 1min →乾燥	0	0	0	0	0	
17	top-Si表面膜ドープ	POCドラフト	80℃ H2O2/H2O2(10%)=500:167(ml) 10min →水洗5min3min →クリーンROXに回収	x	x	0	0	0	
18	リンガラス除去	HFドラフト	H2O:BHF=570:30 (ml) →水洗1min →乾燥	x	x	0	0	0	
19	シート抵抗測定	四端子計	*Swateで計測	1 2 3 4 5 □/□ 55.8 56.8 55.9 56.9 55.9					
20	SH洗浄	SHドラフト	H2SO4(99%)H2O2(10%)=500:167(ml) 10min →水洗5min3min →クリーンROXに回収	0	0	0	0	0	
21	膜厚測定	分米エリプソ			1 2 3 4 5 SiO2 2.8n 2.8n 2.7n 2.9n 2.8n Si 30.3n 30.1n 32.8n 29.1n	x	x	x	
22	チャネルレジスト露光	スピナーコーター	180℃ 3min →HMDS塗布 レジレ1 →450℃ 15min →450℃ 180℃ レジレ2(2000μm→4000μm) →105℃ 3min 条件出し ペア5 Na1.46x35.40x50 KUDO_B15TEST_1204.1 KUDO_B15H_1204.1 KUDO_B15C_1304.1 Dose10 KUDO_B15REF_1204.1	0	0	0	0	0	
23	チャネル露光	H1700	本番 Not-4 条件出し ペア5 Na1.46x35.40x50 KUDO_B15TEST_1204.1 KUDO_B15H_1204.1 KUDO_B15C_1304.1 Dose10 KUDO_B15REF_1204.1	Dose 38	Dose 43	Dose 47	Dose 50	Dose 50	
24	チャネルレジスト露光	H1700ドラフト	180℃ ベーク 1min →CO2 35 Sec →水洗 1min →乾燥	0	0	0	0	0	
25	チャネルレジストイシュー調整	SEM							
26	装置 SO2 除去	HFドラフト	H2O:BHF=570:30 (ml) →水洗1min	0	0	0	0	0	
27	チャネルエッチング	ECR	Nb3+ CD=40 (cc/cm) 52mTorr= 50W 2min5sec (over 30sec)	0	0	0	0	0	
28	チャネルレジスト除去(1段階目)	Asher	Nb3+ 4 CD=8 (cc/cm) 1.6mTorr= 30W 15sec (over 5sec) CD= 500um 10min	0	0	0	0	0	
29	チャネルレジスト除去(2段階目)	SHドラフト	H2SO4(99%)H2O2(10%)=500:167(ml) 10min →水洗5min3min →乾燥	0	0	0	0	0	
30	チャネルレジスト調整	SEM							

31	チャネルの酸化	Siドランプ+Hドランプ	H ₂ O 120℃150% NH ₃ 120℃420/180/9 ml 30min 80℃ →乾燥 30min 3min	0	0			
32	膜厚測定	分光エリプソメ	膜厚化前 膜厚化後 top-Si 38.2h 29.5h	0	0			
33	インプラズマクリーン酸化膜形成	RCA洗浄	水洗5min 3min →80℃ H ₂ O2 (150%) NH ₃ (28%) =1680/720.36 (ml) 10min →水洗5min 3min →HF (50%) H ₂ O =100/1300 (ml) 1min →水洗5min 3min →乾燥	0	0			
34		poly-Si酸化炉	100℃ O ₂ =24ml 4min No.2 ベア基板 →500のクリーンROXに搬す →レジストROXに移動	SiO ₂ 9.3h Si 20.7h	0			
35	インプラズマクレンジスト膜希	スピンドーター	180℃ 3min →HMDS薬液 レンビ1 →50℃ 10min →54.00/14.87 レンビ6 →105℃ 1min	0	0			
36	インプラズマクレンジ	HU700	本番 No.1-2 KUDO, B15RL, 1204.2 KUDO, B15C, 1204.2 Dose30 KUDO, B15REF, 1204.1	dose 40	dose 40			
37	インプラズマクレンジスト膜	H,700ドランプ	105℃ベーク 1min →CD=26 8min →乾燥 1min →乾燥	0	0			
38	インプラズマカバタン膜	SEM観察						
39	ソースドレイン イオン注入	イオン注入装置	Al 4e15/cm ²	0	0			
40	インプラズマクレンジスト膜去(原膜)	Asher	H ₂ SO ₄ (95%) H ₂ O2 (150%) =500/167 (ml) 30min →水洗5min 3min →乾燥	0	0			
41	インプラズマクレンジスト膜去(原膜)	Siドランプ	水洗5min 3min →80℃ H ₂ O2 (150%) NH ₃ (28%) =1680/720.36 (ml) 10min →水洗5min 3min →乾燥	0	0			
42	RCA洗浄	UPCO膜ドランプ	水洗5min 3min →80℃ H ₂ O2 (150%) NH ₃ (28%) =1680/720.36 (ml) 10min →水洗5min 3min →乾燥	0	0			
43	アニール	poly-Si酸化炉	850℃ H ₂ =33min 10min	0	0			
44	チャネルカバタン膜							
45	カーボンコート	poly-Si酸化炉	850℃ O ₂ =24ml 30sec	0	0			
46	カーボンコート	SiPM, UPVO	750℃ SiH ₄ /C ₂ H ₄ =10/110ccm 100min	0	0			
47	膜厚測定	SEM						

48	コンタクトホール電板レジスト塗布	スピコンナー	180℃ 3min →HMDS塗布 レンビ1 →180℃ 2min →ZEP520A レンビ4(500nm) →180℃ 10min 本番 Not-4	0	0	0	0	0	0
49	コンタクトホール電板	HL700	Do800 KU00 B15RL1204.3 KU00 B15C1204.3 Do510 KU00 B15RP1204.1	0	0	0	0	0	0
50	コンタクトホールレジスト塗板	HL700ドラフト	キレン 8min →PA 1min →水洗 1min →乾燥 →150℃ 3min	0	0	0	0	0	0
51	コンタクトホール電板	光學顕微鏡		0	0	0	0	0	0
52	コンタクトホールレジストエッチ(露出目)	HL700ドラフト		0	0	0	0	0	0
53	コンタクトホールレジストエッチ(露出目)	HL700ドラフト		0	0	0	0	0	0
54	コンタクトホールレジスト除去	SHドラフト	H2SO4(95%):H2O(2:30%→500:157(ml)) 10min →水洗5min+3min →乾燥	0	0	0	0	0	0
55	コンタクトホールレジスト電板	光學顕微鏡		0	0	0	0	0	0
56	コンタクトホールレジスト電板	真空蒸着装置	600nm 90℃ 制御波 10min →PA 15min →水洗5min+3min	0	0	0	0	0	0
57	ハブリ洗浄	リターンドラフト		0	0	0	0	0	0
58	AI電板露光レジスト塗布	スピコンナー	薬液 180℃ 3min →HMDS塗布 レンビ1 →180℃ 2min →ZEP520A レンビ4(500nm) →180℃ 10min 薬液 180℃ 3min →HMDS塗布 レンビ1 →180℃ 2min →ZEP520A レンビ4(500nm) →150℃ 1min	0	0	0	0	0	0
59	AI電板露光	HL700	本番 Not-4 Do825 KU00 B15RL1204.4 KU00 B15C1204.4	0	0	0	0	0	0
60	AI電板レジスト塗板	HL700ドラフト	105℃ ベーク 5min →concentrate developer 15min →水洗 1min →乾燥	0	0	0	0	0	0
61	AI電板レジストリターン電板	光學顕微鏡		0	0	0	0	0	0
62	AI電板エッチング	HL700ドラフト	HPO4:HNO3:CH3COOH:H2O=500:34:100:34ml 13min →水洗5min+3min →PA 15min →水洗5min+3min	0	0	0	0	0	0
63	AI電板レジスト除去	HL700ドラフト	90℃ 制御波 10min →PA 15min →水洗5min+3min	0	0	0	0	0	0
64	AI電板リターン電板	光學顕微鏡		0	0	0	0	0	0
65	HMDS処理	真空蒸着	400 CH2-N2-0.52min 10min	0	0	0	0	0	0

公表論文

- (1) “Fabrication of Si Nanowire Field-Effect Transistor for Highly Sensitive, Label-Free Biosensing”
Takashi Kudo, Toshihiro Kasama, Takeshi Ikeda, Yumehiro Hata, Shiho Tokonami, Shin Yokoyama, Takamaro Kikkawa, Hideo Sunami, Tomohiro Ishikawa, Masato Suzuki, Kiyoshi Okuyama, Tetsuo Tabei, Kensaku Ohkura, Yasuhisa Kayaba, Yuichiro Tanushi, Yoshiteru Amemiya, Yoshinori Cho, Tomomi Monzen, Yuji Murakami, Akio Kuroda, and Anri Nakajima
[Japanese Journal of Applied physics, **48**, 06FJ04-1 - 06FJ04-4 \(2009\).](#)
- (2) “Highly sensitive ion detection using Si single-electron transistors”
Takashi Kudo and Anri Nakajima
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- (3) “Biomolecule detection based on Si single-electron transistors for highly sensitive integrated sensors on a single chip”
Takashi Kudo and Anri Nakajima
[Applied Physics Letters, **100**, 023704-1 - 023704-3 \(2012\)](#)
- (4) “Biomolecule detection based on Si single-electron transistors for practical use”
Anri Nakajima, Takashi Kudo and Sadaharu Furuse
[Applied Physics Letters, **103**, 043702-1 - 043702-4 \(2013\).](#)
- (5) “Characteristics of metal–oxide–semiconductor field-effect transistors with a functional gate using trap charging for ultralow power operation”
Takashi Kudo, Takashi Ito, and Anri Nakajima
[Journal of Vacuum Science & Technology B, **31**, 012206-1 - 012206-7 \(2013\).](#)
- (6) “Functional gate metal-oxide-semiconductor field-effect transistors using tunnel injection/ejection of trap charges enabling self-adjustable threshold voltage for ultralow power operation”
Anri Nakajima, Takashi Kudo, and Takashi Ito
[Applied Physics Letters, **98**, 053501-1 - 053501-3 \(2011\).](#)

Fabrication of Si Nanowire Field-Effect Transistor for Highly Sensitive, Label-Free Biosensing

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We fabricated a biosensor based on a silicon nanowire field-effect transistor (SiNW FET) with a Si₃N₄ gate insulator for highly sensitive detection of target biomolecules. The fabricated SiNW FET acted as an ion-sensitive FET that could detect the charge density in solutions flowing

along the gate surface by responding to the pH of the solutions. The SiNW FET also detected charged protein molecules in solution, suggesting that our device can be used in highly sensitive, label-free biosensing.

1. Introduction

The detection and quantification of biological and chemical species are central to many areas of healthcare and the life sciences, ranging from the diagnosis of disease to the discovery of new drug molecules. Field-effect transistors (FETs) are sophisticated devices for detecting charged molecules. Ion-sensitive FETs (ISFETs), which were first reported by Bergveld,¹⁾ change their electrical characteristics in response to the concentration and type of ions present in aqueous solutions on the gate insulator surface. Recently, biosensors and biochips based on FETs have been developed for detecting proteins, DNA, and viruses.²⁻⁷⁾ These methods measure charge changes accompanied by specific molecular recognition events on the gate insulator surface of FETs. Since FETs are fabricated using standard semiconductor technology, many FET sensors can be integrated on a single chip for simultaneous detection and quantification of various biomolecules. To date, a set of ISFETs that measures pH and sodium ion concentration simultaneously⁸⁾ and a biosensor composed of arrayed nanowire FET sensors⁹⁾ have been reported. Nanowire FETs are substantially more sensitive than conventional FETs because electrons or holes in a very narrow channel are more efficiently affected by charges on the gate insulator than those in a wide channel. Therefore, nanowire FETs are suitable candidates for use

in highly sensitive, label-free biosensing. However, since FETs cannot recognize specific molecules themselves, specific recognition elements such as antibodies and enzymes must be immobilized on the gate insulator surface. The immobilization of such biomolecules has been accomplished mainly by the formation of covalent bonds between functional groups on protein molecules (e.g., -NH_2) and complementary coupling groups (e.g., aldehydes or epoxides) introduced onto the solid surfaces. These methods, however, require chemical modification of the surface, and may decrease the binding activity of the immobilized biomolecules because of denaturation by the chemical treatment. To overcome this difficulty, we employed a silicon-binding protein, designated as a “Si-tag”, which strongly binds to silicon dioxide (SiO_2) surfaces¹⁰⁾ as a binder between gate insulator and biomaterials. The active region of the Si-tag always faces away from the SiO_2 surface. The Si-tag can immobilize biomolecules on a SiO_2 layer of a silicon wafer without chemical modification of the surface.^{11, 12)} In this study, however, we used a silicon nitride (Si_3N_4) layer as a gate insulator because of the presence of the leakage path through the SiO_2 layer.¹³⁾ To increase sensitivity, we reduced the Si_3N_4 film thickness to 19 nm, which is extremely thin compared with that of previous works.⁷⁾ Our final goal was to construct FET sensor arrays with biomolecules immobilized via Si-tags on the gate insulator as

molecular recognition elements for rapid, highly sensitive, label-free biosensing. In this study, we fabricated a silicon nanowire (SiNW) FET and investigated its capacity to detect the electric charge of target molecules.

2. Experimental Procedure

We fabricated an n-channel ISFET on a silicon-on-insulator (SOI) wafer using standard semiconductor technology. The thicknesses of the top Si layer (p-type, $10\ \Omega\cdot\text{cm}$) and buried oxide layer of the SOI were 72-76 nm and 400 nm, respectively. The fabrication procedure was as follows.

- (1) The thickness of the top Si layer of the SOI wafer was reduced to 30 nm by oxidation at 1000 °C.
- (2) The SiO_2 on the top Si layer of the SOI was removed by wet-etching.
- (3) A mask pattern of the SiNW was formed by electron-beam lithography with a negative resist (SAL-SR2). The top Si layer of the SOI was etched with the mask pattern using an electron cyclotron resonance etcher. Figure 1 shows a scanning electron micrograph of the fabricated structure after etching. The dimensions of the SiNW were approximately $5\ \mu\text{m} \times 80\ \text{nm} \times 17$

nm (length \times width \times height).

(4) The source and drain areas were formed by ion implantation of As⁺ at 20 keV with a dose of $5 \times 10^{14} \text{ cm}^{-2}$.

(5) Stacked gate insulators were fabricated by two procedures. SiO₂ with a thickness of 10 nm was thermally grown at 850 °C in a dry atmosphere followed by the deposition of 42 nm-thick Si₃N₄ by low-pressure chemical vapor deposition at 750 °C for pH measurement. In addition, we fabricated a thin gate insulator (19 nm Si₃N₄/8 nm SiO₂) for monitoring protein charge.

(6) After wet-etching to form contact holes, Al electrodes were formed and postmetallization annealing was carried out at 400 °C under a hydrogen atmosphere for 30 min.

Figure 2 shows a schematic diagram of our measurement system. A fluidic channel was made of poly(dimethylsiloxane) (PDMS). The volume of the cell was as follows: the size of the fluidic channel on the FET was approximately 3 mm \times 1 mm \times 100 μm (length \times width \times height). The whole area of the FET including the Al pad electrodes (1.0 mm²) was 33.0 mm². The joining surface of the fluidic channel was modified by O₂-plasma treatment, and then attached to the SiNW FET. An Ag/AgCl reference electrode was used to control the gate voltage of the ISFET through a buffer solution. The electrical characteristics were measured using a semiconductor

parameter analyzer (Agilent B1500A).

3. Results and Discussion

3.1 *pH sensing*

First, we investigated the electrical characteristics of the fabricated SiNW FET in the presence of buffer solutions of different pH on the Si₃N₄ gate insulator. Figure 3 shows the drain current (I_{DS}) versus gate voltage (V_G) characteristics obtained in the forward and reverse sweeps. The drain-source voltage (V_{DS}) was fixed at 100 mV. We used the following three solutions: 10 mM tetraborate, pH 9; 50 mM phosphate, pH 7; and 50 mM phthalate, pH 4. The threshold voltage was shifted in the positive (negative) direction with increasing (decreasing) pH of the solution with a shift of 60 mV/pH, which is in good agreement not only with the theoretical value (58 mV/pH, 20 °C) obtained using the Nernst equation but also with previous experimental results (46 ~ 56 mV/pH).^{8, 14)} In addition, the hysteresis was extremely small. The pH response of the I_{DS} of the SiNW FET at a fixed V_G is shown in Fig. 4. The flow rate was 25 μ l/min. When the buffer solution was changed from pH 7 \rightarrow 4 \rightarrow 7 (pH 7 \rightarrow 9 \rightarrow 7), the I_{DS} at a V_{DS} of 100 mV and a V_G of 800 mV increased (decreased) in response to pH. The response time was 400 to 800 s. The changes in the I_{DS} were accurately reproduced. These

results show that the fabricated SiNW FET has reproducibility of pH response and the capacity to detect changes in Si₃N₄ surface potential.

3.2 Detection of protein charges

Next, we investigated the response of the SiNW FET to electrical charges of a protein in solution. We used Si-tags, which are highly positively charged proteins, as a sample. For detection of charged molecules by FET, the Debye length should be longer than the size of the target; otherwise, counter ions in the solution shield the charge of the target. The Debye length b is given by

$$b = \left(\frac{e^2}{\epsilon_o \epsilon_r k T} \sum_i n_i z_i \right)^{-1/2}, \quad (1)$$

where e is the elementary electric charge, ϵ_o and ϵ_r are the vacuum permittivity and relative permittivity of water, respectively, k is the Boltzmann constant, and T is the absolute temperature of the system. n_i and z_i are the concentration and charge of the primary ion i in the solution, respectively. In this study, we prepared the Si-tag solution (30 nM Si-tag in 20 ml of 1 mM tetraborate buffer, pH 9), in which each Si-tag molecule had a positive charge of about $+30e$.

Using the above equation, the Debye length of this solution is calculated to be about 7 nm. Since the size of each Si-tag is estimated to be about 3 nm, the Si-tags immobilized on the Si_3N_4 surface of a FET were within the Debye length. Figure 5 shows the change over time of I_{DS} at a V_{DS} of 100 mV and a V_{G} of 400 mV during successive introduction of the buffer solution, the Si-tag solution, and the buffer solution into the microfluidic channel. First, only the tetraborate buffer was injected into the microfluidic channel, and then, the Si-tags dissolved in tetraborate buffer were injected. When the Si-tags arrived at the SiNW, the drain current increased. The response time was about 50 s. While the Si-tags were flowing along the fluidic channel, the drain current stayed at an increased current level because the positive charge of the Si-tags reduced the surface electric potential. The amplitude drift was about 25 mV while the Si-tags were flowing along the SiNW. This result indicates that the distance between the Si-tags and the Si_3N_4 surface was smaller than the Debye length, as expected, and that the charge of Si-tag molecules in the detection range (i.e., in the distance of the Debye length from the Si_3N_4 surface) was successfully detected by the SiNW FET. However, after the Si-tag solution passed the gate insulator, the increased drain current value gradually returned to its baseline level. Assuming that the diffusion of the Si-tags at the interface between the solution containing the Si-tags and the

buffer solution is ignored, Si-tags were present on the gate surface for 150 s since the flow rate and the volume of the Si-tag solution were 8 $\mu\text{l}/\text{min}$ and 20 μl , respectively. If Si-tags did not bind to the Si_3N_4 surface for this period, the increased drain current would decrease as rapidly as it initially increased. The gradual decrease in I_{DS} suggests that at least some of the Si-tag molecules bound to the Si_3N_4 surface, and that the bound Si-tags gradually dissociated from the surface, probably because of a relatively low affinity for Si_3N_4 . From the result shown in Fig. 5, we calculated the dissociation rate constant k of Si-tags, which is given by

$$I_{\text{DS}} = (I_{\text{DS},0} - I_{\text{DS},\infty})e^{-k(t-t_0)} + I_{\text{DS},\infty} \quad , \quad (2)$$

where t is the measurement time, t_0 is the time at which Si-tags start to dissociate from the Si_3N_4 surface and I_{DS} , $I_{\text{DS},0}$, and $I_{\text{DS},\infty}$ are the drain currents at t , t_0 , and $t = \infty$, respectively. Assuming $t_0 = 200$ s, $I_{\text{DS},0} = 13.1$ nA, and $I_{\text{DS},\infty} = 11.3$ nA from Fig. 5, we obtained a value of $k = 9.0 \times 10^{-3} \text{ s}^{-1}$.

Immobilizing biomolecules using Si-tags on the gate insulator and detecting the corresponding charge may be possible during the dissociation of Si-tags by improving the measurement method and/or measurement system (e.g., by changing the flow rate and shortening the watercourse).

It is noted that the detection of 5 nM m-antibiotin has been achieved using a biotin-modified

SiNW FET.¹⁵⁾ The sensitivity of our SiNW FET may increase to an equivalent level by narrowing the width of the SiNW.

4. Conclusions

We fabricated a SiNW FET with a $\text{Si}_3\text{N}_4/\text{SiO}_2$ stack gate insulator on an SOI wafer using semiconductor fabrication technology. The threshold voltage of the fabricated SiNW FET changed with the pH of the solution on the gate insulator with a shift of about 60 mV/pH, which is consistent with the theoretical value obtained using the Nernst equation. We also demonstrated real-time detection of highly positively charged Si-tag proteins, which bind to SiO_2 surfaces and can be used for immobilization of biomolecules on SiO_2 surfaces. Our device detected the Si-tag molecules flowing along the channel. However, our results suggest that Si-tags have lower affinity for Si_3N_4 than for SiO_2 . We are currently developing a SiNW FET with a $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ stack gate insulator for efficient immobilization of biomolecules using Si-tags to improve our biosensing system.

Acknowledgment

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Fig. 1. Scanning electron micrograph of fabricated silicon nanowire (width: 80 nm).

Fig. 2. Schematic diagram of measurement system.

Fig. 3. Drain-source current (I_{DS}) vs. gate voltage (V_G) characteristics of Si nanowire field-effect transistor in presence of three buffer solutions on the gate insulator surface. The drain-source voltage (V_{DS}) was fixed at 100 mV.

Fig. 4. Change over time of drain-source current (I_{DS}) during sequential injection of three buffer solutions of different pH. The drain-source voltage (V_{DS}) and gate voltage (V_G) were fixed at 100 and 800 mV, respectively.

Fig. 5. Change over time of drain-source current (I_{DS}) during injection of Si-tag solution into fluidic channel. The drain-source voltage (V_{DS}) and gate voltage (V_G) were fixed at 100 and 400 mV, respectively.

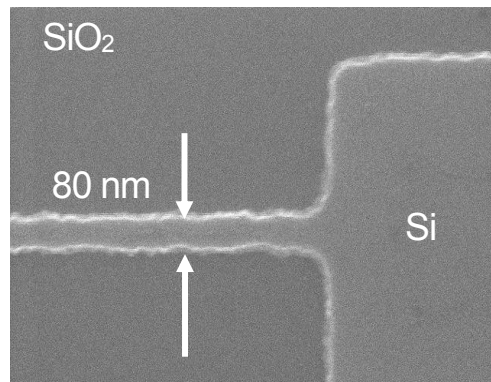


Fig. 1

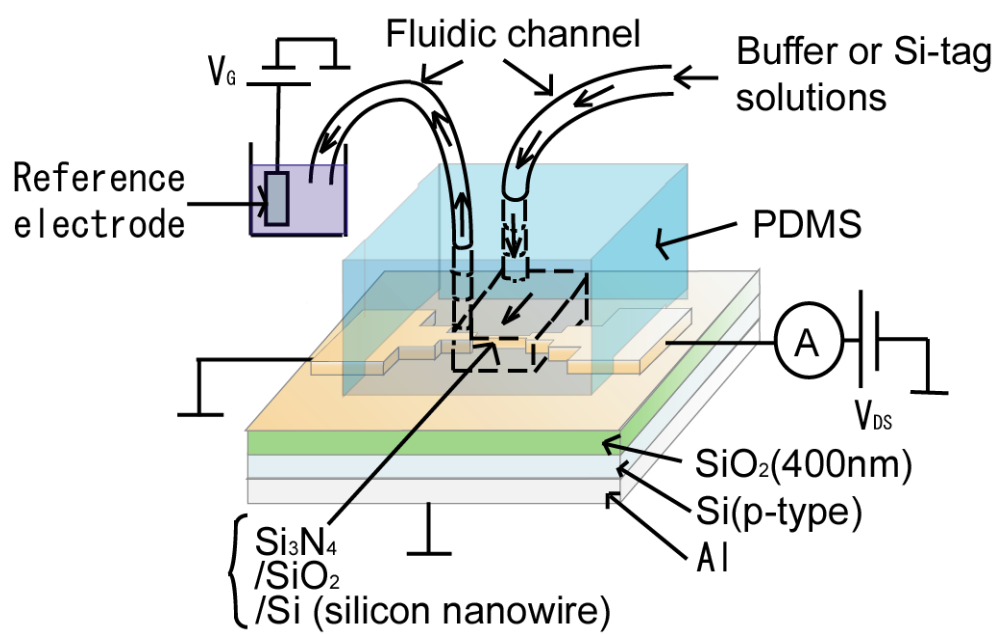


Fig. 2

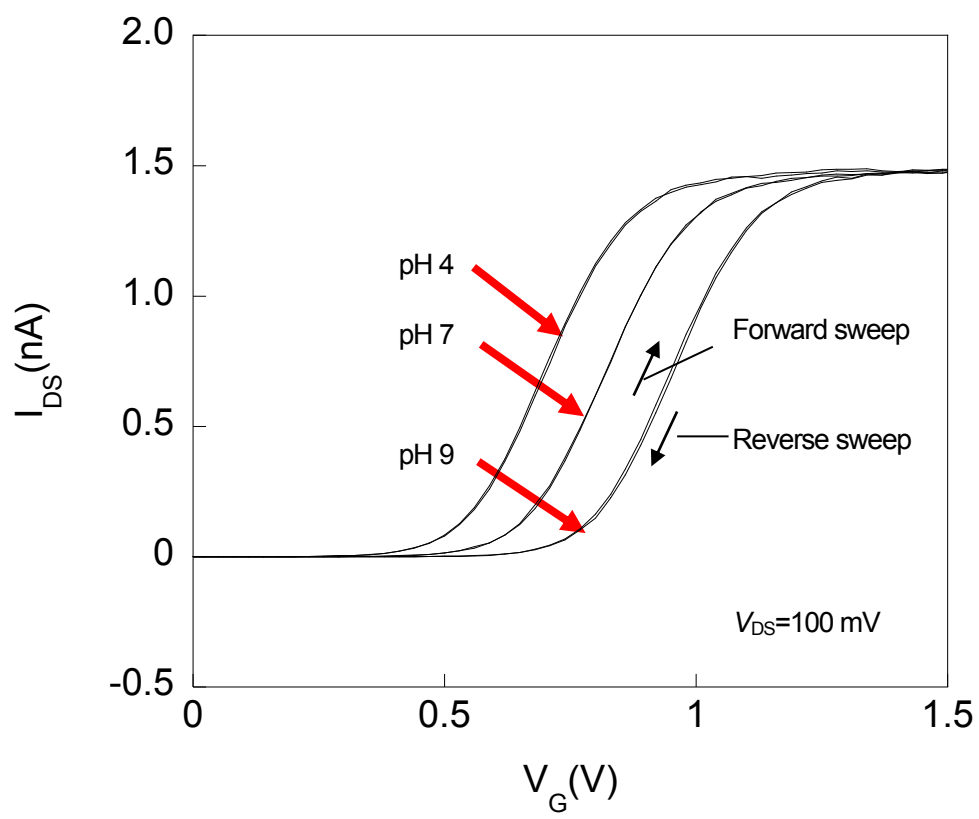


Fig. 3

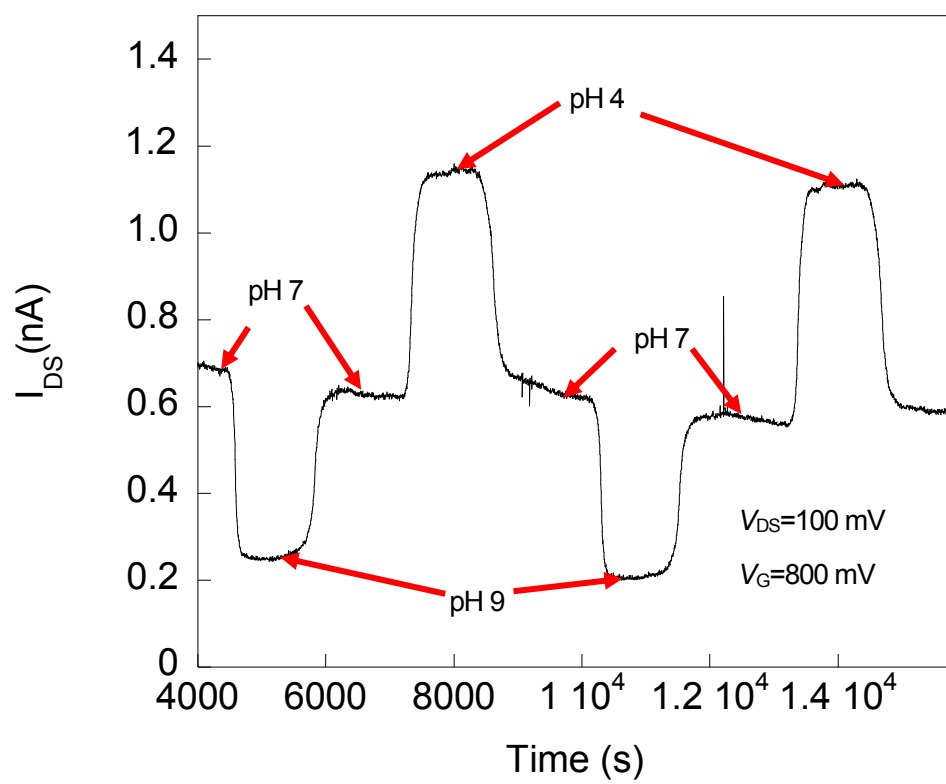


Fig. 4

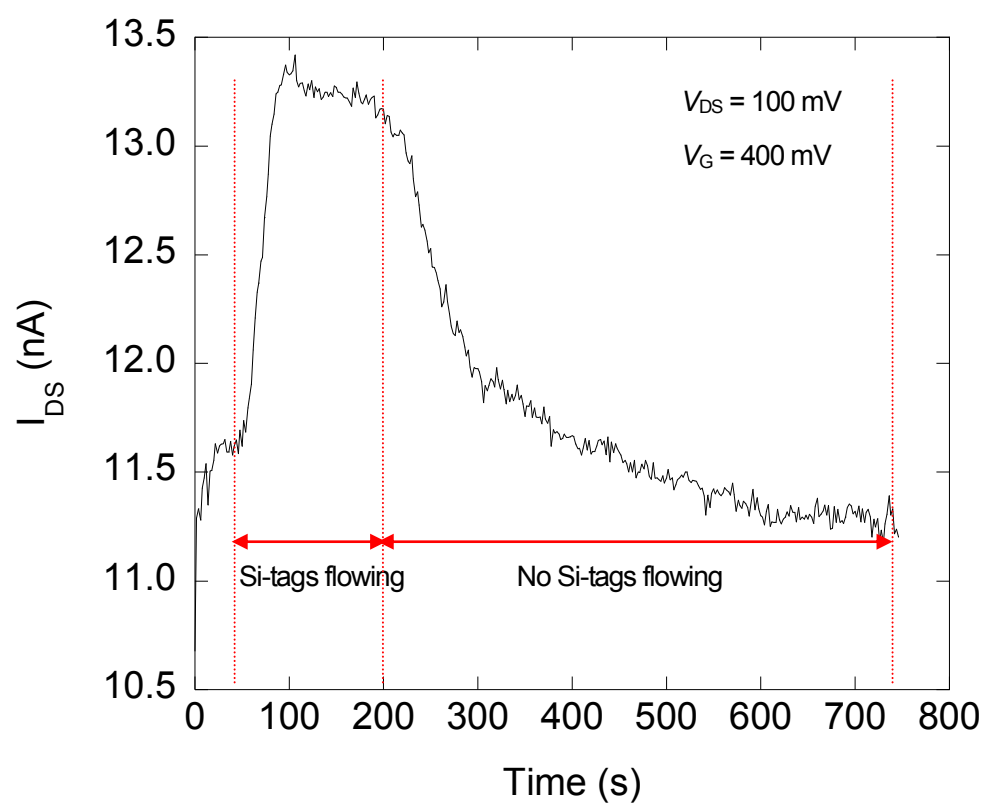


Fig. 5

Highly sensitive ion detection using Si single-electron transistors

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Si single-electron transistors (SETs) were used for highly sensitive ion detection. A multiple-island channel structure was adapted in the SET for room-temperature operation. Clear Coulomb oscillation and diamonds were observed at room temperature. Using the Coulomb oscillation, clear pH responses of drain current (I_d)-gate voltage (V_g) characteristics were obtained despite the existence of I_d noise. Because Coulomb oscillations have a possibility to increase the slope of I_d over V_g near the half-maximum current of the peaks, high resolving power of ion, and/or biomolecule concentration can be expected. A Si-structure will make it possible to integrate the sensors on a single chip. © 2011 American Institute of Physics. [doi:10.1063/1.3569148]

The detection and quantification of chemical and biological species are central to many areas of healthcare and the life sciences, ranging from the diagnosis of disease to the discovery of new drug molecules. Field effect transistors (FETs) are sophisticated devices used for the detection of charged molecules.¹ Ion-sensitive FETs change their electrical characteristics in response to the concentration and type of ions present in aqueous solutions on the gate insulator surface. Furthermore, biosensors, and biochips based on FETs have recently been developed for the detection of DNA, proteins, and viruses.²⁻⁹ These methods are used to measure changes in charge accompanied by specific molecular recognition events on the gate insulator surface of FETs. High sensitivity in detecting target ions or biomolecules has been obtained using nanowire channels in FET sensors.⁹⁻¹¹ However, FET sensors with even higher sensitivity in detecting targets are preferable, especially in dilute solutions of targets, where large noise exists in the drain current (I_d)-gate voltage (V_g) characteristics. Therefore, we have proposed a FET sensor utilizing a single-electron transistor (SET) for highly sensitive ion and/or biomolecule detection. High resolving power of ions and/or biomolecule concentration can be expected using Coulomb oscillation. Since room-temperature operation is necessary for ion and/or biomolecule sensing, a multiple-island system is effective for SETs. Moreover, a Si-structure is important since we can use existing large scale integration (LSI) technology in the fabrication, and the fabricated FET sensors can be integrated on a single chip for simultaneous detection and quantification of various ions and/or biomolecules. Therefore, in this study, we fabricated a Si SET sensor with multiple islands for highly sensitive pH detection (one type of ion detection) and demonstrated its fundamental electrical characteristics.

We fabricated a one-dimensional array of nanoscale islands in a silicon-on-insulator (SOI) layer by using electron beam lithography. There were 11 islands, and the channel length was 3 μm . We used a p-type (B doped) SOI (100) wafer (13.5–22.5 $\Omega \cdot cm$). No channel doping was performed. The device fabrication process is as follows. After the etching of the island array with an electron cyclotron resonance

etcher using the resist pattern as a mask, subsequent isotropic wet etching in an $NH_4OH/H_2O_2/H_2O$ solution¹² was carried out to reduce the dimensions of the array [Fig. 1(a)]. Next, the oxidation was carried out to further reduce the size of the islands and the width of the wire regions, which act as tunnel barriers for electrons. The final island size and wire width was about 50 nm and 30 nm, respectively. The final thickness of the top-Si was about 18 nm. After the source and drain areas were formed by ion implantation of As^+ at 30 keV with a dose of $4 \times 10^{15} \text{ cm}^{-2}$, we fabricated Si_3N_4/SiO_2 stacked gate insulators as follows. A layer of SiO_2 about 9 nm thick was thermally grown at 850 $^\circ C$ in a dry atmosphere followed by the deposition of about 36 nm thick Si_3N_4 by low-pressure chemical vapor deposition at 750 $^\circ C$.

A schematic diagram of our measurement system is shown in Fig. 1(b). A fluidic channel was made of polydimethylsiloxane (PDMS). The volume of the cell was as follows: the size of the fluidic channel on the FET was approximately 3 mm \times 1 mm \times 100 μm (length \times width \times height). The entire area of the SET including the Al pad electrodes

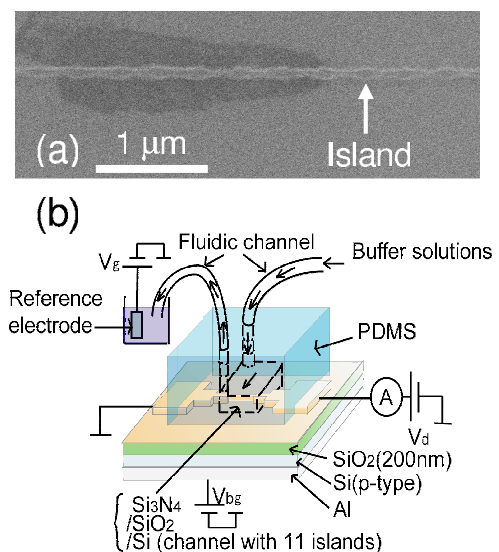


FIG. 1. (Color online) (a) Scanning electron micrograph (SEM) of the channel region of the fabricated Si SET with 11 islands after dry and wet etching. The dark area is due to a long time high resolution SEM observation. (b) Schematic diagram of measurement system.

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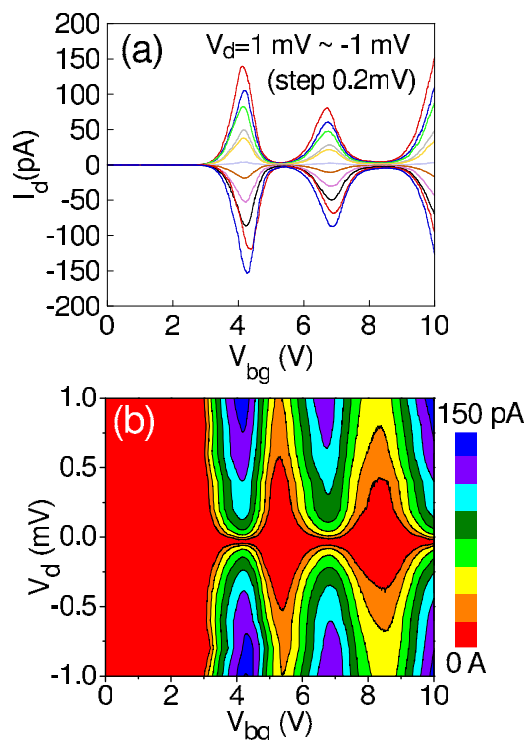


FIG. 2. (Color online) (a) Drain current (I_d) vs back-gate voltage (V_{bg}) characteristics as a function of drain-source voltage (V_d) at room temperature for the fabricated SET with 11 islands. V_d from -1 to 1 mV in V_d steps of 0.2 mV. (b) Contour plot of I_d as a function of V_d and V_{bg} at room temperature. Devices with larger dot size and barrier width did not show Coulomb oscillations.

(0.25 mm^2) was 1.2 cm^2 . The joining surface of the PDMS was modified by O_2 plasma treatment and then attached to the SET. An Ag/AgCl reference electrode was used to control the V_g of the SET through a buffer solution. The electrical characteristics were measured using a semiconductor parameter analyzer (B1500A, Agilent).

First, we investigated the electrical characteristics of the fabricated SET under the absence of buffer solutions on the $\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked gate insulators. In this measurement, the gate voltage was applied through the backside of the device (Si substrate of the SOI wafer). Figure 2(a) plots I_d versus back-gate voltage (V_{bg}) characteristics at room temperature. The drain-source voltage (V_d) was varied from -1 to 1 mV in V_d steps of 0.2 mV. Two peaks of Coulomb oscillation were confirmed around $V_{bg} = 4$ and 7 V. Figure 2(b) shows the contour plot of I_d as a function of V_d and V_{bg} evaluated from Fig. 2(a). Clear Coulomb diamonds were observed. The positions of the two peaks of Coulomb oscillation in Fig. 2(a) correspond to the constricted parts in Fig. 2(b). Therefore, room-temperature SET operation was confirmed for the fabricated devices. The high temperature operation is thought to have been achieved due to a serially connected multiple-island system as discussed later.

Figure 3 plots the I_d versus V_g characteristics at a V_d of 1 mV for three different buffer solutions: 50 mM phthalate, $\text{pH } 4$; 50 mM phosphate, $\text{pH } 7$; and 10 mM tetraborate, $\text{pH } 9$. In this measurement, the reference electrode in the buffer solutions was used as a gate while keeping $V_{bg} = 0$ V. We confirmed a linear relationship between the solution potential and V_g ($0 < V_g < 2$ V) with a slope close to one, indicating no electrochemical reactions took place in

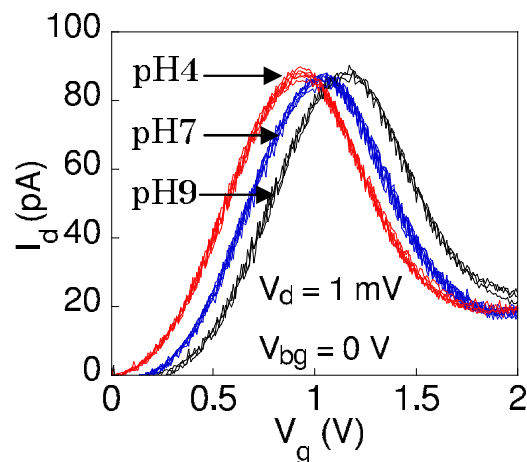


FIG. 3. (Color online) Drain current (I_d) vs gate voltage (V_g) characteristics of the SET with 11 islands for three different pH values at room temperature. The drain-source voltage (V_d) was fixed at 1 mV. The back-gate voltage (V_{bg}) was also fixed at 0 V. The leakage current between the reference electrode and source/drain contact is very small and keeping the value within 2 pA less than the noise level at the V_g range from 0 to 2 V, ensuring the measurement reliability.

solution at the V_g range. The flow rate of the solutions was $0.1 \mu\text{l/min}$. The buffer solution was changed from $\text{pH } 4 \rightarrow 7 \rightarrow 9 \rightarrow 7 \rightarrow 4$ to confirm the reproducibility of the pH response. For every pH change, I_d - V_g measurements were carried out three times to investigate the stability under a constant pH. Both in the increase in pH ($\text{pH } 4 \rightarrow 7 \rightarrow 9$) and the decrease in pH ($\text{pH } 9 \rightarrow 7 \rightarrow 4$), the I_d - V_g curves for the same pH coincide well. The small hysteresis (threshold voltage shift less than 5 mV) insures the high resolution pH detection. As can be seen in the figure a clear Coulomb oscillation peak was observed for each pH value. The peak position varied with the pH of the buffer solution. For $V_g > 2$ V, we did not carry out measurements due to the large leakage currents between the reference electrode and back-gate (typically about 3 nA at $V_g = 2$ V). Because there was no peak in Coulomb oscillation for $V_g < 0$ V in Fig. 3, this peak is assumed to correspond to the first peak of Coulomb oscillation (around 4 V of V_{bg}) in Fig. 2(a).

A summary of the pH response characteristics of the SET is plotted in Fig. 4. Because there is some noise in the measured I_d - V_g curves in Fig. 3, each measured I_d - V_g curve of Coulomb oscillation was fitted using a least-squares pro-

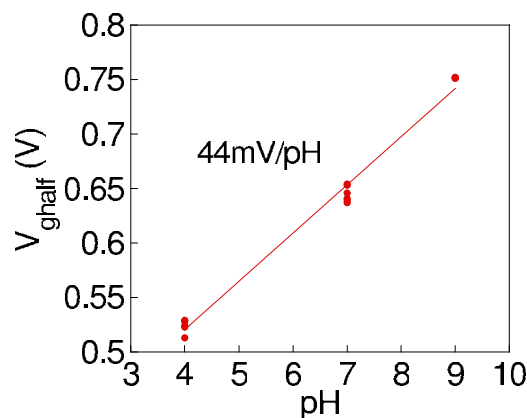


FIG. 4. (Color online) pH response characteristics of the fabricated SET with 11 islands at room temperature.

gram, and the V_g values were obtained at the left side half-maximum current of each fitted curve in order to precisely evaluate the pH sensitivity. The obtained V_g value ($V_{g\text{ half}}$) was shifted in the positive (negative) direction as the pH of the buffer solution was increased (decreased). The slope of the calibration curve ($V_{g\text{ half}}$ versus pH curve) is about 44 mV/pH, which agrees well with previous experimental results (46–56 mV/pH).¹³ The slight difference in our experimentally obtained value and the theoretical value (58 mV/pH, 20 °C) may be due to the oxygen content in the Si_3N_4 layer.¹³ These results show that reproducible pH responses were obtained with the fabricated SET.

The possible advantage of using SETs as ion and/or biomolecule sensors is as follows. In an SET, Coulomb oscillations with a symmetry shape and the same peak height appear when the barrier conductance is constant in the whole V_g regions according to the orthodox theory.¹⁴ However, when the dependence of barrier conductance on V_g exists, Coulomb oscillations are modulated and weighted by the variation in the barrier conductance. Therefore, if the barrier conductance increases with V_g , it is possible that the final slope of I_d over V_g in the SET becomes larger than that of the barrier itself. Especially in SETs with barriers consisted of semiconductor nanowires with low doping level, this situation can occur and the slope can be larger than that of the nanowire itself. In such a case, the largest slope can be obtained around a V_g near the left side half-maximum current of the peaks in SETs. Under conditions where large I_d noise exists, the larger slope of I_d over V_g leads to a better resolving power of ion and/or biomolecule concentration. Also, there is an advantage of utilizing SETs to evaluate the target concentration value from only the change in I_d at $V_g=0$ V. In this case, there is a merit that it is not necessary to sweep V_g for searching a threshold voltage (V_{th}). For that purpose, conventional metal-oxide-semiconductor field-effect transistors with highly doped channel were generally used in accumulation to measure the I_d change at a fixed V_g of 0 V for the pH detection. However, in accumulation highly doped channel shows the metal like conduction: the slope of I_d over V_g is small. Accordingly, it is difficult for V_{th} change with a small pH change to be detected if relatively large I_d noise exists, leading to the difficulty in high resolution pH detection. Instead, if we use an SET pH sensor with highly doped channel region including Coulomb islands and barriers, high resolution pH detection becomes possible due to the Coulomb oscillation: the slope of I_d over V_g becomes larger. This leads to the merit of high resolution pH detection without sweeping V_g .

For ion and/or biomolecule sensing, room-temperature operation is strongly required. To achieve room-temperature operation of an SET with a single island, the island, and junction sizes should be reduced to less than 10 nm in order to reduce the total capacitance.¹⁵ However, it is difficult to fabricate such structures reproducibly by using currently available LSI fabrication techniques. One way to overcome the difficulty is to utilize serially connected islands instead of a single island. In such a multiple-island system, the effective total capacitance of each island decreases compared with that in a single-island system because the junction capaci-

ties are connected in series.^{15,16} This leads to an increase in the charging energy of each island and to an increase in the operation temperature. In other words, to enable room-temperature operation, a multiple-island system can use a larger island than that used by a single-island system. Moreover, SETs with serially connected islands can suppress cotunneling,¹⁷ which increases the valley current of Coulomb oscillation and prevents higher temperature operation.¹⁸ To date, we have applied an SET with multiple islands connected in series to an exclusive-OR (XOR) circuit, which achieved room-temperature operation.¹⁹ Therefore, we used the multiple-island system to realize room-temperature operation of an SET for highly sensitive pH sensing in this study. In fact, we were not able to obtain Coulomb oscillations at room-temperature in SETs with a single-island system in this study.

In summary, we fabricated a Si SET with multiple islands for pH sensors integrated on a single chip. Clear Coulomb oscillations and Coulomb diamonds were confirmed at room temperature. Clear pH responses of I_d - V_g characteristics were obtained by using Coulomb oscillations despite the existence of I_d noise. The slope of the calibration curve was 44 mV/pH. Because Coulomb oscillations have a possibility to increase the slope of I_d over V_g near the half-maximum current of the peaks, a Si SET sensor with multiple islands is promising for future high sensitivity ion and/or biomolecule sensors integrated on a single chip.

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Biomolecule detection based on Si single-electron transistors for highly sensitive integrated sensors on a single chip

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Biomolecule detection was achieved using a Si single-electron transistor (SET) for highly-sensitive detection. A multiple-island channel-structure was used for the SET to enable room-temperature operation and to increase sensitivity. Coulomb oscillation shifted against the gate voltage due to biotin-streptavidin binding. Coulomb oscillation has a possibility to increase transconductance (g_m), and a higher g_m leads to greater sensitivity to a charged target. Since a Si structure is important for integrating label-free-biomolecule and/or ion sensors into large-scale-integrated circuits, a Si SET with multiple islands should enable the integration of a sensor system on a single chip for multiplexed detections and simultaneous diagnoses. © 2012 American Institute of Physics. [doi:10.1063/1.3676664]

The detection and quantification of chemical and biological species are central to many areas of healthcare and life sciences. Field effect transistors (FETs) are sophisticated devices used for the label-free detection of charged molecules.¹ Ion-sensitive field effect transistors (ISFETs) are a typical example. Furthermore, biosensors based on FETs have recently been developed for the detection of DNA, proteins, and viruses.^{2–7} FETs measure changes in charge accompanied by specific molecular recognition events on the gate insulator surface. Highly sensitive detection of target ions or biomolecules has been obtained using a nanowire channel in FET sensors.^{8–11} However, FET sensors with even higher detection sensitivity are preferable, especially for dilute solutions of targets, which have relatively high electrical noise levels.

Single electron transistors (SETs) are a promising candidate for highly sensitive detection because using Coulomb oscillations has a possibility to result in high resolving power for ion and/or biomolecule concentrations. Owing to the difficulties in room temperature (RT) operation of SETs, there have been no reports of an SET-based biosensor.

We previously developed a pH sensor based on a Si SET with a multiple-island channel structure for ion detection.¹² It operates effectively at RT. We have now developed a biomolecule sensor based on a Si SET that also has a multiple-island channel structure. We clarified the advantages of a multiple-island structure and proved the feasibility of highly sensitive biomolecule and ion sensors. The Si structure enables the use of existing large-scale integration (LSI) technology for chip fabrication. The fabricated FET sensors can be integrated on a single chip for simultaneous detection and quantification of various ions and/or biomolecules.

We fabricated SETs with multiple Coulomb islands serially connected in a silicon-on-insulator (SOI) layer. They have 11 islands and a channel length of 3 μm . The fabrica-

tion process and device structure are similar to those of our previously reported ISFET using a Si SET (Ref. 12) with a slight modification. A p-type (B-doped) SOI (100) wafer (8.5–11.5 Ωcm) was used. The thicknesses of the top silicon layer and buried oxide on the SOI wafers were 50 and 400 nm, respectively. Doping of the top silicon layer was carried out by POCl_3 diffusion at 850 $^\circ\text{C}$ for 30 min. The doping level was about $3.5 \times 10^{20}\text{cm}^{-3}$. The fabrication process of a channel region includes electron beam lithography and dry etching using an electron-cyclotron resonance etcher with the resist pattern as a mask. Subsequent isotropic wet etching in a solution of $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ at 80 $^\circ\text{C}$ reduced the dimensions of the device, and the damage introduced during the dry etching process.¹³ The nanowire region (constricted region in the channel) acts as a tunnel barrier due to the quantum-size effect.¹⁴ A scanning electron micrograph of the channel region of a fabricated Si SET with 11 islands after dry etching is shown in Fig. 1(a).

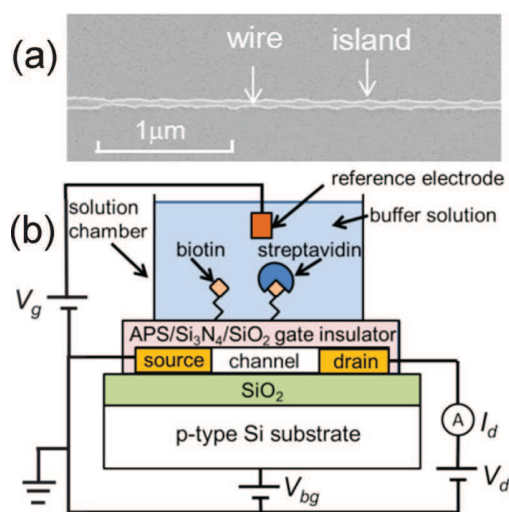


FIG. 1. (Color online) (a) Scanning electron micrograph of fabricated Si single-electron transistor (SET) with 11 islands after dry etching. (b) Schematic diagram of measurement system.

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Next, we fabricated $\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked gate insulators. A layer of SiO_2 , about 10 nm thick, was thermally grown at 850 °C in a dry atmosphere followed by the deposition of about 90-nm-thick Si_3N_4 by low-pressure chemical vapor deposition at 750 °C. The final thickness of the top Si layer was estimated to be about 35 nm (excluding the thickness of the SiO_2). The final width of the nanowire barrier region was about 10 nm and the length was 150–200 nm. The wider region of the island width was about 30 nm and the island length was 50–100 nm. After contact holes and Al electrodes were fabricated, the samples were annealed at 400 °C in an H_2 atmosphere.

A schematic diagram of our measurement system is shown in Fig. 1(b). A solution chamber was attached to the $\text{Si}_3\text{N}_4/\text{SiO}_2$ gate insulator. The channel region including all barriers and islands in the SET was inside the solution chamber region. The diameter of the chamber was 0.5 cm. An Au reference electrode was used to control the gate voltage (V_g) of the SET through a buffer solution.

The $\text{Si}_3\text{N}_4/\text{SiO}_2$ gate insulator surface was chemically modified. To remove organic contamination, the surface of the Si_3N_4 layer was cleaned in a solution of $\text{H}_2\text{O}/\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ (weight ratio of 18:1:1) at 80 °C for 10 min.¹⁵ After being rinsed with pure water, the surface was cleaned again with 1 M NaOH for 1 h at RT.⁷ To silanize the Si_3N_4 surface [i.e., to form an aminopropylsiloxane (APS) surface], the surface was soaked in 2 wt.% 3-aminopropyltriethoxysilane (APTES) in anhydrous toluene⁷ at 60 °C for 10 min. It was then rinsed in anhydrous toluene and dried immediately in vacuum at 110 °C for 1 h.⁷ After silanization, biotin (250 $\mu\text{g}/\text{ml}$) was reacted with the APS-terminated Si_3N_4 surface at RT for 30 min to obtain a biotinylated surface. Finally, the biotinylated surface was reacted with 10- $\mu\text{g}/\text{ml}$ streptavidin for 30 min. The electrical characteristics were measured using a semiconductor parameter analyzer (B1500A, Agilent).

Figure 2 shows the results of biomolecule detection using the well-known ligand-receptor binding of biotin-streptavidin. To avoid the problem of Debye screening, we chose the ion concentrations in the buffer solution such that the Debye screening length was sufficiently long to enable detection and sufficiently short to screen unbound biomolecules.¹⁶ At the same time, the pH of the buffer solutions was set to 8.0–8.2 since the isoelectric point of streptavidin is pH 5–6.¹⁰ Therefore, the streptavidin was negatively charged in the buffer solution. The drain current (I_d)-gate voltage (V_g) characteristics were measured before and after the biotinylation of the APS-terminated surface and after the subsequent addition of 10- $\mu\text{g}/\text{ml}$ streptavidin to the biotinylated surface. For each surface modification, the electrical characteristics were obtained five times to confirm reproducibility. As can be seen in Fig. 2(a), the I_d - V_g curve differed for each surface modification. For the reason described later, we evaluated the V_g shift in each curve on the left side of the peak. At the half-maximum peak current, the V_g value ($V_{g\text{ half}}$) shifted –220 mV due to the attachment of biotin to the APS-terminated surface, which is consistent with the positive charge of biotin [Fig. 2(b)]. In contrast, the successive addition of 10- $\mu\text{g}/\text{ml}$ streptavidin resulted in an increase in $V_{g\text{ half}}$ (the V_g shift = +150 mV), which is consistent with the negative charge of streptavidin. If we fixed the V_g (=5.95 V)

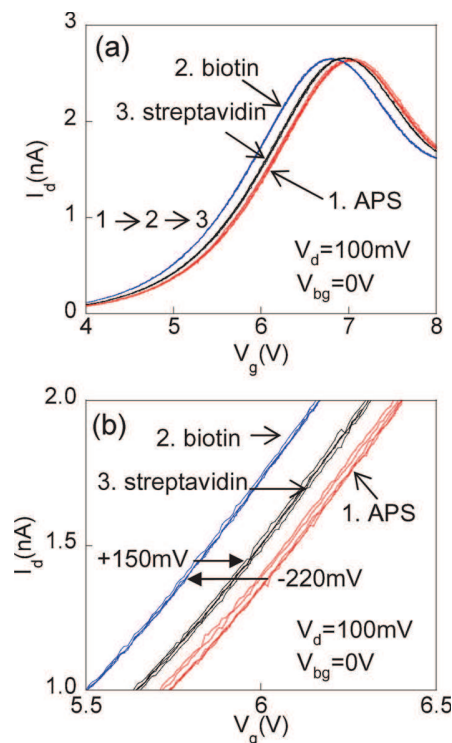


FIG. 2. (Color online) Drain current (I_d) vs. gate voltage (V_g) characteristics of SET with multiple islands for biotin-streptavidin binding at room temperature. Drain-source voltage (V_d) was fixed at 100 mV. Back-gate voltage (V_{bg}) was fixed at 0 V. The results were for 10- $\mu\text{g}/\text{ml}$ streptavidin. (b) Curves in V_g region from 5.5 to 6.5 V for (a).

at $V_{g\text{ half}}$ for APS-terminated surface, we can observe correspondingly that I_d increases (the average I_d shift = +350 pA) after the attachment of biotin and then decreases (the average I_d shift = –220 pA) after the successive binding of streptavidin. These experimental results demonstrate the achievement of biomolecule detection based on a Si SET using the binding of biotin-streptavidin.

The advantage of the use of an SET for biomolecular and/or ion sensing is as follows. If the barrier conductance (drain conductance) depends on V_g , the Coulomb oscillations are modulated and weighted by the variation in the barrier conductance. If the barrier conductance increases with V_g , the transconductance (g_m) in the SET possibly becomes larger than that of the barrier itself [Fig. 3(a)]. In this case, g_m can be larger, especially around a left-side V_g value near the half-maximum peak current. A larger g_m leads to higher sensitivity to a charged target. If SETs with a sufficiently doped channel were used in accumulation mode, there is an advantage that targets can be detected only from the change in I_d at $V_g = 0$ V (it is not necessary to increase V_g). When MOSFETs with a sufficiently doped channel were used in accumulation mode, a metal-like conduction appeared, in which the drain conductance was almost constant against V_g . However, such a MOSFET cannot be used for biomolecule detection because $g_m = 0$ [Fig. 3(b)]. Even in this case, if the channel structure was changed to that of an SET, Coulomb oscillation appeared, and g_m increased [Fig. 3(b)]. In the inversion mode, the advantage of detecting targets at $V_g = 0$ V cannot be obtained usually due to the high threshold voltage (V_{th}).

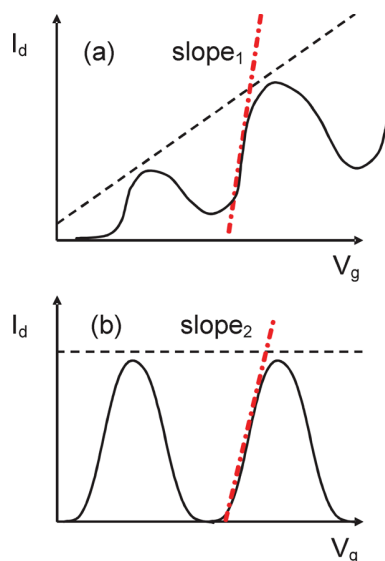


FIG. 3. (Color online) Schematic view illustrating reason for highly sensitive detection of charged target when SET was used for case in which barrier conductance (drain conductance) increases with gate voltage (V_g) (a) and for case in which barrier conductance was constant (b). Broken lines show drain current vs. gate voltage characteristics of nanowire barrier region. Dash-dotted lines show steepest slope of drain current (I_d) against V_g .

Using a multiple-island channel structure in SETs has two advantages for biomolecular and/or ion sensing. One is high-temperature operation. For ion and/or biomolecule sensing, RT operation is strongly required. To achieve RT operation of an SET with a single island, the island size should be less than 10 nm, which is difficult even with present LSI technologies.¹⁷ A serially connected multiple-island channel structure overcomes this difficulty because the effective total capacitance of an island decreases, which leads to an increase in the charging energy.^{14,17,18} The other advantage is that the multiple-island system increases the sensitivity: I_d in the SET easily changes with the dilute target concentration because it changes even if only one target molecule attaches to one of the islands (Fig. 4). Receptor molecules on the island surfaces are attached by surface modifications. If a target molecule happens to meet with one of the receptor molecules, specific binding occurs, and the effective gate voltage in the SET changes, leading to a change in the drain current. The probability of a target molecule meeting a receptor molecule is larger in a multiple-island channel structure than in a single-island channel structure.

In summary, biomolecule detection was achieved using a Si single-electron transistor for highly sensitive detection. After chemical modification of the $\text{Si}_3\text{N}_4/\text{SiO}_2$ gate insulator surface with 3-aminopropyltriethoxysilane and biotin, streptavidin was detected on the basis of a clear shift in the gate voltage at the half-maximum peak current of the Coulomb

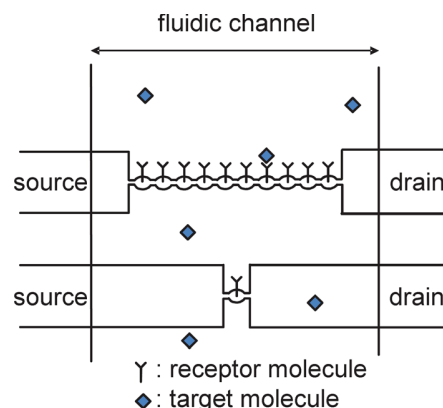


FIG. 4. (Color online) Schematic view illustrating reason for highly sensitive detection of charged target by using multiple-island channel structure.

oscillation. Coulomb oscillation has a possibility to increase the transconductance (g_m), and a larger g_m leads to higher sensitivity to a charged target. A channel structure with serially connected islands can operate at room temperature and has higher sensitivity. Since a Si structure enables label-free-biomolecule and/or ion sensors to be integrated into an LSI chip, a Si SET with multiple islands should enable the integration of a sensor system on a single chip for multiplexed detections and simultaneous diagnoses.

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Biomolecule detection based on Si single-electron transistors for practical use

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Experimental and theoretical analyses demonstrated that ultra-sensitive biomolecule detection can be achieved using a Si single-electron transistor (SET). A multi-island channel structure was used to enable room-temperature operation. Coulomb oscillation increases transconductance without increasing channel width, which increases detection sensitivity to a charged target. A biotin-modified SET biosensor was used to detect streptavidin at a dilute concentration. In addition, an antibody-functionalized SET biosensor was used for immunodetection of prostate-specific antigen, demonstrating its suitability for practical use. The feasibility of ultra-sensitive detection of biomolecules for practical use by using a SET biosensor was clearly proven through this systematic study. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4816267>]

Detection and quantification of chemical and biological species are central to many areas of healthcare and life sciences, ranging from the diagnosis of disease to the discovery of drug molecules. Field effect transistors (FETs) are sophisticated devices used for the label-free detection of charged molecules.^{1–8} Highly sensitive detections of target ions or biomolecules were reported using nanowire channels in FET sensors.^{9–16} However, FET sensors with even higher detection sensitivity are required, especially when the target molecules are dilute in concentration. Since the high detection sensitivity of nanowire FET sensor is due to the suppression of leakage current in drain current (I_d) from the percolation paths through the channel at a dilute concentration of target species in solution,^{17–19} to obtain even higher sensitivity, the transconductance (g_m) should be increased without increasing the channel width. Another approach is needed to achieve this.

Single-electron transistors (SETs) are a promising candidate for achieving even higher detection sensitivity due to their Coulomb oscillations. There were no reports of a SET-based ion sensor or biosensor except our recent publications^{20,21} probably due to the difficulty of room temperature operation of SETs. Using a Si multi-island channel structure, we recently developed a pH SET sensor²⁰ and a biomolecule SET sensor (“SET biosensor”) for biotin-streptavidin binding²¹ and reported the preliminary experimental results at a relatively high concentration. We have now performed a systematic study, including both experimental and theoretical analyses, of the SET biosensor. We have clarified the mechanism of ultra-sensitive detection with a SET biosensor and have developed an advantageous strategy for using it. A biotin-modified SET biosensor was used to detect streptavidin at a dilute concentration. Using a SET sensor, we also demonstrated immunodetection of prostate-specific antigen

(PSA; a protein biomarker of prostate cancer), demonstrating the practicality of the sensor: The detected PSA concentration was 4 ng/ml, which is the target detection level for practical use.

We fabricated Si SETs with multiple serially connected Coulomb islands in a silicon-on-insulator (SOI) wafer [Figs. 1(a) and 1(b)]. Such a configuration is advantageous for room-temperature SET operation because it increases the probability of existence of an extremely small island and/or reduces the effective junction capacitance of an island. The number of island is 11. Smaller numbers of island tend to increase the island size due to the proximity effect of wide source/drain regions in the electron beam (EB) lithography. On the other hand, larger numbers of island tend to increase the probability of disconnection in the narrow wire regions. Highly doped channel structure was adopted in this study to operate in the accumulation mode. The final thickness of the channel region was less than 20 nm. The final island and wire widths were less than 20 nm and 10 nm, respectively. The nanowire region acts as a tunnel barrier. The length of channel is 3 μm . The channel region including all barriers and islands in the SET was inside the solution chamber region. The diameter of the chamber was 0.5 cm. An Au reference electrode was used to control the gate voltage (V_g) of the SET through a buffer solution. The process flow of the accumulation-mode SET fabrication is as followed.^{22–24} The thickness of the buried oxide on the used B-doped SOI (100) wafers was 400 nm. Doping (n-type) of the top silicon layer was carried out by POCl_3 diffusion at 850 °C for 30 min. The doping level was about $3.5 \times 10^{20} \text{ cm}^{-3}$. The fabrication process of a channel region includes EB lithography and dry etching. Subsequent isotropic wet etching in a solution of $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ reduced the dimensions of the device and the damage introduced during the dry etching process.²⁵ Next, a $\text{Si}_3\text{N}_4/\text{SiO}_2$ stacked gate insulator was fabricated: A layer of SiO_2 , about 10 nm thick, was thermally grown followed by the deposition of about 90-nm-thick Si_3N_4 by using low-pressure chemical vapor deposition. After contact holes and Al electrodes were fabricated, the samples were

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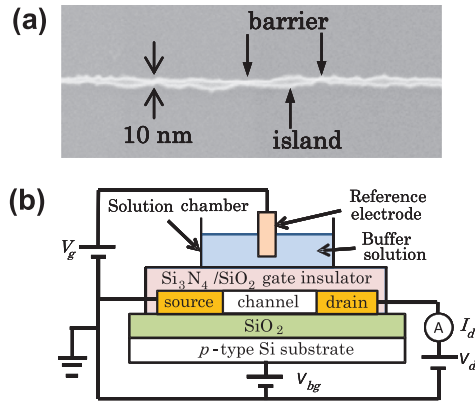


FIG. 1. Device structures. (a) Scanning electron micrograph of fabricated Si SET with 11 islands after dry and wet etching. (b) Schematic diagram of measurement system.

annealed at 400 °C in an H₂ atmosphere. Then, a solution chamber was attached to the Si₃N₄/SiO₂ gate insulator.

Chemical modification of the Si₃N₄/SiO₂ gate insulator surface for the biotinylated one is as follows. First, to remove organic contamination, the surface of the Si₃N₄ layer was cleaned in a solution of H₂O/H₂O₂/NH₄OH (weight ratio of 18:1:1) at 80 °C for 10 min.²⁶ After being rinsed with deionized water, the surface was cleaned again with 1 M NaOH for 1 h at RT.⁶ To amino-silanize the Si₃N₄ surface [i.e., to form an aminopropylsiloxane (APS) surface], the surface was soaked in 2 wt. % 3-aminopropyltriethoxysilane (APTES) in anhydrous toluene⁶ at 60 °C for 10 min. It was then rinsed in anhydrous toluene and dried immediately in vacuum at 110 °C for 1 h.⁶ After amino-silanization, biotin (250 μg/ml) was reacted with the APS-terminated Si₃N₄ surface at room temperature (RT) for 30 min to obtain a biotinylated surface.

Chemical modification of the gate insulator surface for the anti-PSA reacted one is as follows. To remove organic contamination, the surface of the Si₃N₄ layer was cleaned in a solution of H₂O/H₂O₂/NH₄OH. After being rinsed with deionized water, the surface was cleaned again with 1 M NaOH for 1 h at RT. To form an APS surface, the surface was soaked in 10 wt. % APTES in anhydrous toluene at RT for 30 min. The amino-silanized Si₃N₄ surface was then rinsed in deionized water and dried immediately in vacuum at 110 °C for 30 min. Next, the amino-silanized Si₃N₄ surface is soaked in a mixed solution (volume ratio of 1:1) of a 25 wt. % glutaric dialdehyde solution with 0.01 g of NaBH₃CN per 1 ml and 250 mM phosphate buffer solution for 4 h at room temperature. Then, the aldehyde-functionalized Si₃N₄ surface is coupled to anti-PSA by reaction of 125 μg/ml anti-PSA in pH 8.4 phosphate buffer solution containing 4 mM NaBH₃CN for 4 h at RT. Finally, the unreacted Si₃N₄ surface aldehyde is blocked by using 50 mM ethanolamine containing 4 mM NaBH₃CN for 10 min.

In nanowire FETs, high detection sensitivity is obtained due to the suppression of leakage current in I_d from the percolation paths through the channel even in the dilute range of target molecule concentration^{17–19} [Figs. 2(a) and 2(b)]. SET biosensors have higher sensitivity than nanowire FET ones because of their Coulomb oscillations, as shown in

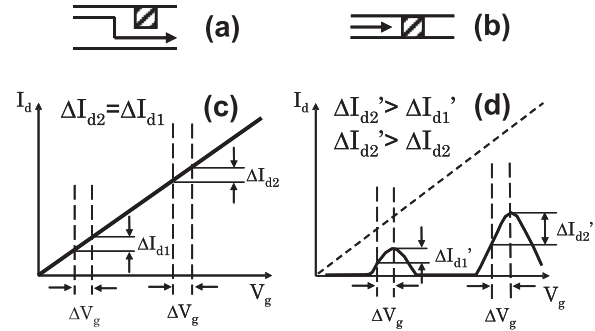


FIG. 2. Schematic views to explain the mechanism of high sensitivity in detection of charged species when a nanowire channel FET and a SET are used. (a) When wide channel is used in a FET, a percolation path exists from the source to the drain. Shaded squares represent charged species. Only the small change of drain current (ΔI_d) can be obtained after the charged species bound to the channel. (b) When a nanowire channel is used in a FET, no percolation path forms, leading to the large ΔI_d . Drain current (I_d)–gate voltage (V_g) characteristics are shown for (c) nanowire FET and (d) SET. ΔV_g is change in gate voltage accompanied by binding of biomolecule. In (d), I_d – V_g characteristics of SET (solid line) was obtained by V_g dependence of I_d for nanowire barrier region (broken line) weighted by Coulomb oscillation.

Figs. 2(c) and 2(d). Here, ΔI_d is the change in I_d , and ΔV_g is that of V_g accompanied by the binding of biomolecules. The larger the ΔI_d for a constant ΔV_g , the higher the sensitivity. In nanowire FETs [Fig. 2(c)], ΔI_d is almost constant or decreases with increasing V_g for a constant ΔV_g . In SETs [Fig. 2(d)], on the other hand, the variation of I_d with V_g for the nanowire barrier region are modulated and weighted by the Coulomb oscillation. This leads to an increase in ΔI_d for a constant ΔV_g at corresponding V_g 's with increasing V_g . Therefore, in principle, the sensitivity in the SET can be higher than that in the nanowire FET.

The I_d – V_g characteristics showed clear Coulomb oscillations for a fabricated SET biosensor in buffer solution at room temperature [Fig. 3(a)]. The overall increase in I_d with V_g is due to the effect of I_d – V_g characteristics of the nanowire barrier region. The gate capacitance C_g of an island was estimated from the periodicity of the I_d peaks to be 0.25 aF. The I_d –drain voltage (V_d) characteristics in the inset showed a clear Coulomb blockade region at the V_g of a valley at room temperature. The junction capacitance C_s ($=C_d$) of the island was estimated from the magnitude of the Coulomb blockade region to be 0.16 aF. As anticipated [Figs. 2(c) and 2(d)], ΔI_d increased with increasing V_g for a constant ΔV_g , as shown in Fig. 3(a), especially at a V_g near the left-side half-maximum of the I_d peaks. This is also cleared by the increase in g_m with increasing V_g [Fig. 3(b)].

The results of theoretical analysis support these findings. The equivalent circuit used for the analysis is shown in the inset of Fig. 4(a). The I_d – V_g characteristics for a SET biosensor (solid curve) were obtained using the I_d – V_g characteristics of a FET having only the nanowire barrier region (broken curve) weighed by the analytical formula for Coulomb oscillation [Fig. 4(a)]. The used analytical formula for Coulomb oscillation is as follows:^{27–29}

$$I_n = \frac{e}{2R_{\Sigma}C_{\Sigma}} \frac{(\tilde{V}_{g,n}^2 - \tilde{V}_d^2) \sinh(\tilde{V}_d/\tilde{T})}{\tilde{V}_{g,n} \sinh(\tilde{V}_{g,n}/\tilde{T}) - \tilde{V}_d \sinh(\tilde{V}_d/\tilde{T})},$$

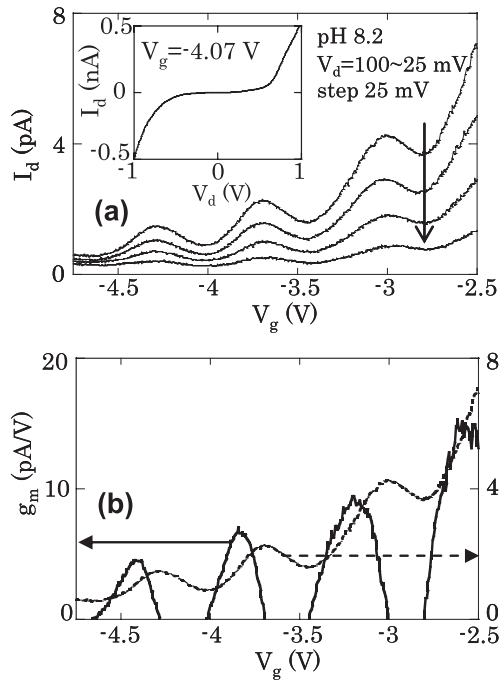


FIG. 3. Experimental results of SET biosensor in buffer solution. (a) Drain current (I_d)–gate voltage (V_g) characteristics. V_g was applied using reference electrode. V_d was varied from 100 to 25 mV in steps of 25 mV. Back-gate voltage (V_b) was fixed at 0 V. The inset shows I_d –drain voltage (V_d) characteristics for valley at V_g of -4.07 V. (b) Transconductance (g_m)– V_g characteristics. I_d – V_g curve for $V_d = 100$ mV was used, and only positive g_m values are shown.

where

$$\tilde{V}_{g,n} = \frac{2C_g V_g}{e} - \frac{(C_g + C_{sub} + C_s - C_d)V_d}{e} - 1 - 2n,$$

$$\tilde{V}_d = \frac{C_\Sigma V_d}{e},$$

$$\tilde{T} = \frac{2k_B T C_\Sigma}{e^2},$$

and

$$R_\Sigma = R_T + R_T,$$

where k_B , e , T , C_g , C_s , C_d , C_{sub} , C_Σ , and n are the Boltzmann constant, elementary charge, temperature, gate capacitance, junction capacitances at source and drain, capacitance between the island and the substrate, total capacitance, and electron number in the island. R_Σ is the resistance of the barrier region, and $R_\Sigma = 2R_T$, where R_T is the resistance of a tunnel junction. T was room temperature; a C_g of 0.25 aF and a $C_s (=C_d)$ of 0.16 aF were used from the results shown in Fig. 3. $C_\Sigma (=C_g + C_{sub} + C_s + C_d)$ was assumed to be 0.6 aF, which is almost the same as that for the SET biosensor for which the results shown in Fig. 3 were obtained. We can see from the calculated results that ΔI_d increases with increasing V_g for a constant ΔV_g at the corresponding V_g 's, especially at a V_g near the left-side half-maximum of the I_d peaks [Fig. 4(a)]. Indeed, g_m was larger in the SET than in the nanowire FET in the large V_g region [Fig. 4(b)]. The I_d reduction due to the effect of correlations in the SET was taken into consideration in the calculation. Namely, an electron must first tunnel off the island before the next one can tunnel on the island in SETs. Therefore, in principle, the sensitivity of a SET can be made much larger than that of a nanowire FET by increasing V_g .

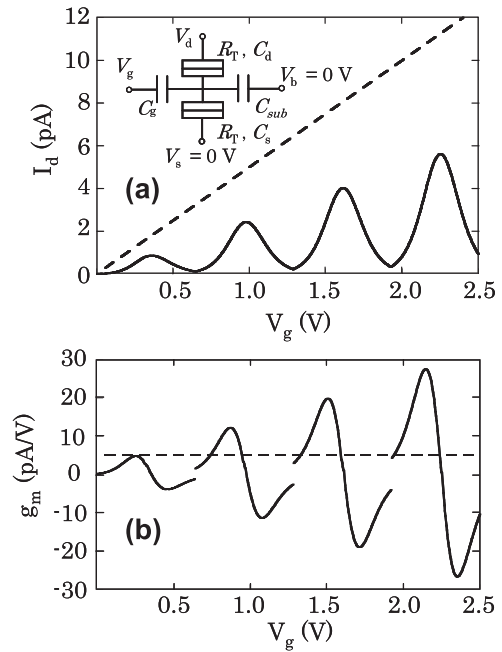


FIG. 4. Theoretical analysis. (a) Analytical curves for drain current (I_d)–gate voltage (V_g) characteristics of a SET. The inset shows the used equivalent circuit. (b) Transconductance (g_m)– V_g characteristics of a SET. In (a), solid curve was calculated using I_d – V_g characteristics for nanowire barrier region (broken curve) weighted by the formula of Coulomb oscillation in text. In (b), solid curve is for SET, and broken curve is for nanowire barrier region. Discontinuities in g_m appear for SET at V_g 's corresponding to minimum I_d 's between adjacent I_d peaks in (a) due to two different n 's at the V_g .

We detected ligand-receptor binding of biotin-streptavidin using a SET biosensor. The I_d – V_g characteristics showed clear Coulomb oscillations [Fig. 5(a)]. The addition of streptavidin to the biotinylated surface resulted in an

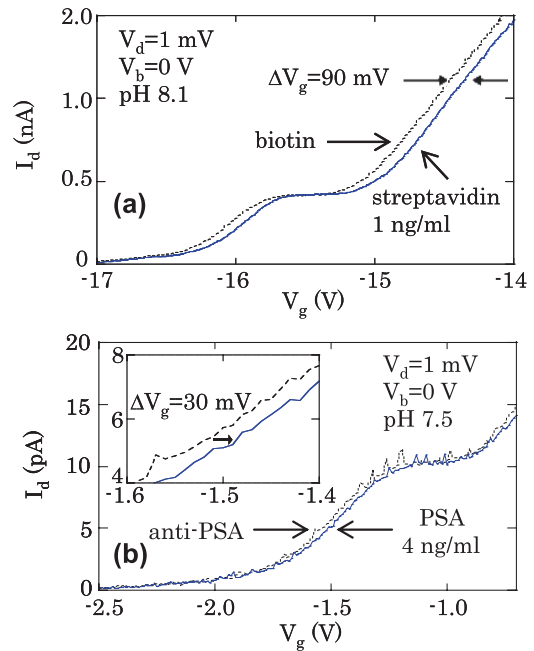


FIG. 5. Drain current (I_d)–gate voltage (V_g) characteristics of SET biosensor. (a) Streptavidin concentration of 1 ng/ml. (b) PSA concentration of 4 ng/ml. The inset shows curves in V_g region from -1.6 to -1.4 V. Problem of Debye screening was avoided by setting ion concentrations in buffer solutions such that Debye screening length was sufficient for detection. Back-gate voltage (V_b) was fixed at 0 V.

increase in threshold voltage (V_{th}), namely, a positive ΔV_g . This is consistent with the streptavidin's negative charge in solution at pH 8.1. We previously reported the detection of streptavidin at a concentration of 10 $\mu\text{g/ml}$.²¹ We have now detected streptavidin binding down to 1 ng/ml (16 pM). The ΔV_g was 90 mV.

Immunodetection of PSA using a SET biosensor was achieved, as shown in Fig. 5(b). The PSA detection level was 4 ng/ml, which is the required detection level for practical use. Due to the isoelectric point (6.9) of PSA, the binding event of PSA to the anti-PSA reacted surface in solution at pH 7.5 is equivalent to the binding of a negative charge. This should result in a positive ΔV_g , which is consistent with the results shown in Fig. 5(b). The ΔV_g was 30 mV.

The feasibility of ultra-sensitive detection of biomolecules by using a Si SET biosensor was clearly proven through this systematic study. Silicon structures are important for LSI integration, and Si SET biosensors open the door to the development of integrated single-chip sensor systems suitable for multiplexed and simultaneous diagnoses.

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Characteristics of metal–oxide–semiconductor field-effect transistors with a functional gate using trap charging for ultralow power operation

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A functional gate metal–oxide–semiconductor field-effect transistor that enables self-adjustment of threshold voltage (V_{th}) was developed for the ultralow power operation. The operating principle enables the on-current to be increased without increasing the off-current. Prototype devices were fabricated with complementary metal–oxide–semiconductor (CMOS) fabrication technology using a silicon-on-insulator substrate, and the fundamental device characteristics necessary for ultralow power operation were demonstrated with an emphasis on the device reliability. A negative V_{th} shift was caused by electron ejection from the poly-Si charge trap layer, and a positive V_{th} shift was caused by electron injection from the top gate electrode. A fabricated device endured 10^5 electron ejection-and-injection cycles when only a positive bias V_g was applied. Endurance characteristics of the fabricated devices showed that the number of cycles to oxide breakdown increased as the channel size decreased. The authors explained the SiO_2 breakdown mechanism by using a percolation model. They consider that scaling down of the channel size and the thickness of the tunnel gate oxide will open the way to the development of CMOS logic applications for this device. © 2013 American Vacuum Society. [<http://dx.doi.org/10.1116/1.4773576>]

I. INTRODUCTION

Extensive effort has been devoted to scaling metal–oxide–semiconductor field-effect transistors (MOSFETs) for low-power-consumption large-scale integrated circuits (LSIs).¹ The use of high- k gate dielectrics has also been intensively studied as a means of power reduction.^{2,3} However, the fundamental difficulty in decreasing the threshold voltage (V_{th}) and/or S -factors (S denotes subthreshold swing) when scaling MOSFETs limits further reduction of the power supply voltage. Since power (P) is proportional to VDD (Ref. 2) (VDD is the power supply voltage), lowering V_{th} by 0.1 V while keeping the gate overdrive voltage the same corresponds to a 20% reduction in power consumption in advanced complementary metal–oxide–semiconductor (CMOS) LSIs. However, lowering V_{th} generally increases the off-current. To avoid this increase, either the S -factor has to be reduced or V_{th} has to be adjusted to a high value in the off-current state and a low value in the on-current state (meaning self-adjustment of V_{th}). To date, tunnel field-effect transistors (FETs),⁴ ferroelectric-gate FETs,^{5,6} and suspended-gate MOSFETs^{7,8} have attracted significant interest as ways to achieve S -factors lower than 60 mV/dec. However, there are still issues with these potential devices in terms of the process cost and compatibility with existing CMOS fabrication technology.

In the previous study, we proposed a MOSFET with a functional gate that enables self-adjustment of V_{th} for low power operation.⁹ A prototype device was fabricated with CMOS technology and preliminary results of the device characteristics were obtained.

In this study, we carried out a systematic study on the fundamental device characteristics necessary for ultralow power logic operation, while putting emphasis of the device reliability by assessing the endurance characteristics of the tunnel and lower gate oxides, their dependence on the scaling of the channel size, and a discussion of the breakdown mechanism. Through the results, we found the way to the development of CMOS logic applications for this device.

II. OPERATION PRINCIPLE

A schematic diagram of fabricated n -channel MOSFET with a functional gate is shown in Fig. 1. The structure of the MOSFET resembles that of the conventional floating gate memory. The only difference is that a thin tunnel gate SiO_2 exists between the floating gate and the top gate electrode in the functional gate. Hereafter, we call “the floating gate” in our logic device a “charge trap layer,” in distinction from memory devices. In the MOSFET, electrons move between the charge trap layer and the top gate electrode through the tunnel gate oxide. The operation principle of the fabricated n -channel MOSFET and band diagram of the functional gate structure are shown in Fig. 2. Initially, no electrons move between the charge trap layer and the top gate electrode because of the charge neutrality in the charge trap layer when the gate voltage (V_g) is sufficiently low (usually $V_g = 0$ V) in the off-state [Fig. 2(a)]. In this case, the off-state current (I_{off}) [in drain current (I_d)] is sufficiently low at the off-state voltage (V_{off}) [$V_g = 0$ V], as shown by curve A in Fig. 2(d). However, the on-state current (I_{on}) also becomes low at the on-state voltage (V_{on}) [curve A of Fig. 2(d)]. On the other hand, when V_g is switched to a large value in curve A, electrons move from the charge trap layer to the top gate electrode [Fig. 2(b)]. Since this leads to an additional lowering of the surface potential of the channel, the V_{th} shifts in

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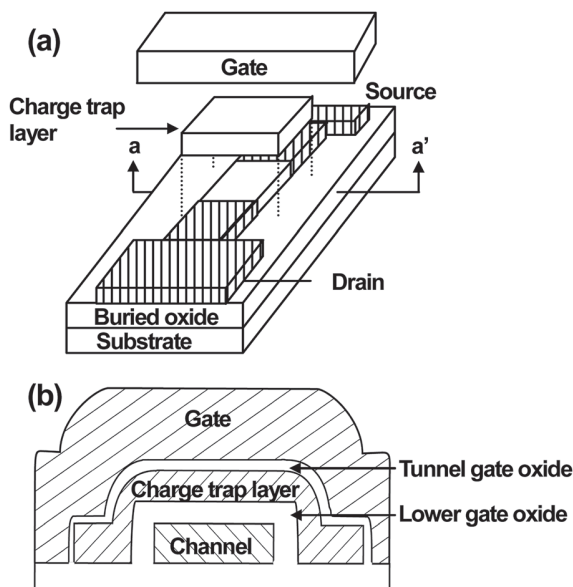


FIG. 1. (a) Schematic diagram of fabricated functional gate MOSFET. The shaded regions are heavily As^+ implanted. (b) Cross-sectional view along a–a' line in (a). Thicknesses of the tunnel gate oxide, lower gate oxide, and Si channel were 2.4, 10, and 60 nm, respectively.

the negative direction and I_{on} increases [curve B of Fig. 2(d)]. Finally, when V_g returns to a low value in curve B [Fig. 2(c)], electrons return from the top gate electrode to the charge trap layer as a result of lowering of the Fermi energy level caused by electron ejection. Therefore, the V_{th} changes back to the positive direction and I_{off} decreases [curve A of Fig. 2(d)]. In this way, the proposed MOSFET can increase I_{on} without increasing I_{off} , and this leads to ultralow power operation.

III. EXPERIMENT

The device fabrication process was a slight modification to that of the floating gate memory previously reported.^{10–12} A p -type (B-doped) silicon-on-insulator (100) wafer was used. Electron beam lithography and dry etching were utilized to define the charge trap layer and channel. The thickness of the Si channel was 60 nm. The channel width (W) and length (L) were changed as follows: $0.5 \mu\text{m} \times 0.5 \mu\text{m}$, $0.7 \mu\text{m} \times 0.7 \mu\text{m}$, $0.8 \mu\text{m} \times 0.8 \mu\text{m}$, and $1.0 \mu\text{m} \times 1.0 \mu\text{m}$, respectively. After defining the channel area and forming the lower gate oxide, an amorphous Si film was deposited for the charge trap layer. Then, the resist mask line was formed parallel to the channel. Dry etching was carried out to define the width of the charge trap layer. The width of the charge trap layer was slightly larger than that of the channel. While the tunnel gate oxide was formed by thermal oxidation, the amorphous Si of the charge trap layer changed to poly-Si. After that, a poly-Si film was deposited for the top gate electrode and doping of the poly-Si was carried out by POCl_3 diffusion. Next, the resist mask line was formed perpendicularly across the channel. This time, the dry etching was stopped upon reaching the lower gate oxide. The lengths of the charge trap layer and the top gate electrode were made the same as that of the channel by using this self-aligned etching process. The thicknesses of the tunnel gate oxide (T_{ox}) and lower gate oxide were 2.4 and 10 nm, respectively. The thickness of the charge trap layer was 70 nm. After the source and drain areas were formed by ion implantation of As^+ at 30 keV with a dose of $4 \times 10^{15} \text{cm}^{-2}$ and annealing, the interlayer dielectrics were deposited. The device fabrication was completed with the formation of Ohmic contacts. The electrical characteristics were measured using a

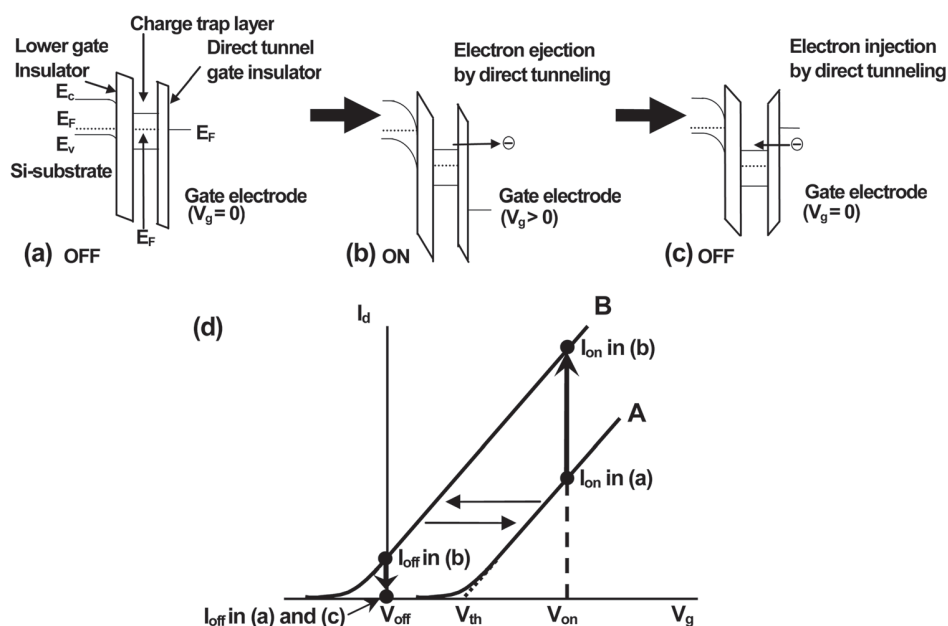


FIG. 2. Band diagrams of functional gate structure of the MOSFET in the off-current and on-current states (a) in the condition of charge neutrality in the charge trap layer, (b) in the case of electrons moving from the charge trap layer to the top gate electrode, (c) in the case of electrons returning from the gate electrode to the charge trap layer. (d) The operating principle of self-adjustment of the threshold voltage (V_{th}) for ultralow power operation of the proposed functional gate MOSFET. E_C , E_V , and E_F are the energies of conduction-band edge and valence-band edge, and Fermi energy level, respectively.

semiconductor parameter analyzer with a pulse generator (4156C and 41501B, Agilent). For the measurements, the electron injection into the charge trap layer was carried out by applying a negative bias V_g with 0 V at the source while keeping the substrate and drain open. On the other hand, the electron ejection was carried out by applying a positive bias V_g with 0 V at the source while keeping the substrate and drain open. I_d - V_g measurements were carried out immediately after electron injection or ejection. It took about 30 s for one I_d - V_g measurement.

IV. RESULTS

Figure 3(a) shows the I_d - V_g characteristics for positive and negative bias V_g applications. Since it is important to evaluate the change of the required gate voltage in the on-current state, I_{onc} was defined as I_d at the V_{th} plus 1.0 V and V_{onc} was defined as V_g at I_{onc} . Accordingly, I_{onc} was 3.7 μ A and V_{onc} was 4.3 V in the initial I_d - V_g characteristics. Note that the gate leakage current (I_{leak}) was less than the noise

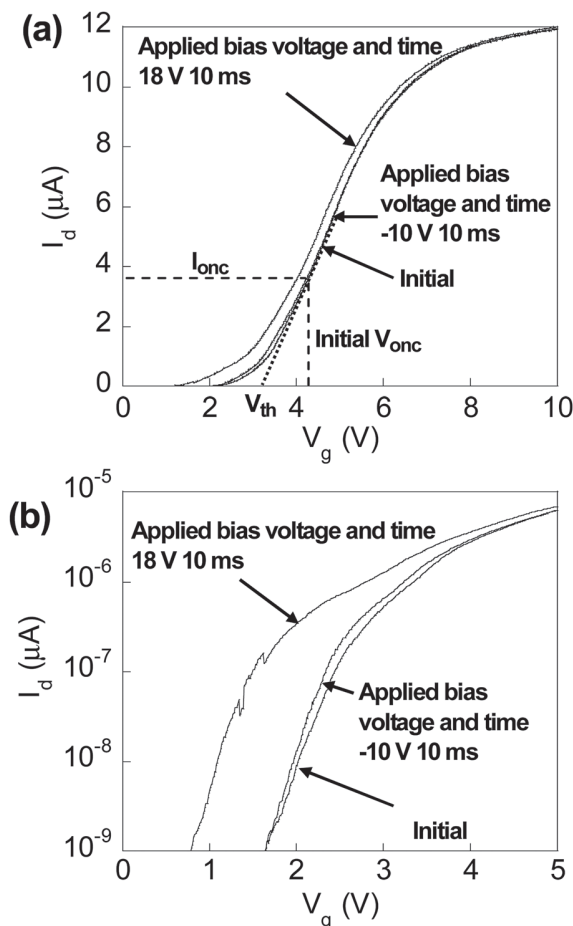


FIG. 3. Bias voltage dependence of drain current (I_d)-gate voltage (V_g) characteristics. Drain voltage (V_d) = 0.1 V. (a) Initial I_d - V_g characteristics and those after a positive bias V_g application (18 V, 10 ms) and those after a subsequent negative bias V_g application (-10 V, 10 ms). The dotted line illustrates the linearly extrapolated threshold voltage (V_{th}) at the initial I_d - V_g characteristics. Broken lines indicate I_{onc} [(defined as I_d at the V_{th} plus 1.0 V] and V_{onc} (defined as V_g at I_{onc}) at the initial I_d - V_g characteristics. (b) Note that the linear scale axis of I_d in (a) has been changed to a log scale in this figure.

level (1 pA) in the V_g range from 0 to 10 V (not shown). After a positive bias V_g of 18 V was applied for 10 ms, V_{onc} shifted to the negative side of the initial V_{onc} value, indicating that electrons were ejected from the charge trap layer. Note that the direction of the V_{onc} shift was opposite to that of conventional floating gate memories. A subsequent negative bias V_g application of -10 V for 10 ms made V_{onc} return to a value close to the initial V_{onc} , indicating that electrons were injected into the charge trap layer. Here, the shift in V_{onc} (ΔV_{onc}) was about -0.25 and 0.22 V after positive and negative bias V_g applications, respectively. These results prove the feasibility of the operation principle of the fabricated MOSFET with a functional gate, which increases I_{on} without increasing I_{off} . In Fig. 3(b), the ordinate axis for I_d is a log scale. Although the reason is not clear yet, the shift in V_g for a constant I_d in the small I_d region ($I_d < 0.5 \mu$ A) was larger than in the large I_d region ($I_d > 0.5 \mu$ A) after the positive and negative bias V_g applications.

Figure 4 shows the dependence of I_d on the drain voltage (V_d) before and after applying a positive bias V_g of 18 V for 10 ms. The device showed typical I_d - V_d characteristics, such as clear I_d saturation at $V_g = 3$ V, before and after the positive bias. Consistent with the results in Fig. 3, I_{on} was indeed larger after the positive bias.

Figure 5(a) shows the I_d - V_g characteristics when a negative bias was not applied after the positive bias. Here, the initial I_{onc} was 3.9 μ A and V_{onc} was 4.3 V in the initial I_d - V_g characteristics. The first I_d - V_g measurement was carried out immediately after a positive bias V_g of 18 V was applied for 10 ms. The initial V_{onc} shifted in the negative direction (ΔV_{onc} was -0.3 V). The second I_d - V_g measurement was carried out immediately after the first one. In this case, V_{onc} changed to the positive direction and returned to a value close to the initial one (the voltage difference between initial V_{onc} and this V_{onc} was slight, 0.03 V). Since it took about 30 s for each I_d - V_g measurement, the time necessary for V_{onc} to return to the initial value ranged from about 30 to 60 s. Figure 5(b) shows the endurance characteristic of this device. Here, V_{low} and V_{high} are defined as the V_{onc} for the first and second I_d - V_g measurements after the positive bias at each cycle, respectively. Both V_{high} and V_{low} increased with the cycle number.

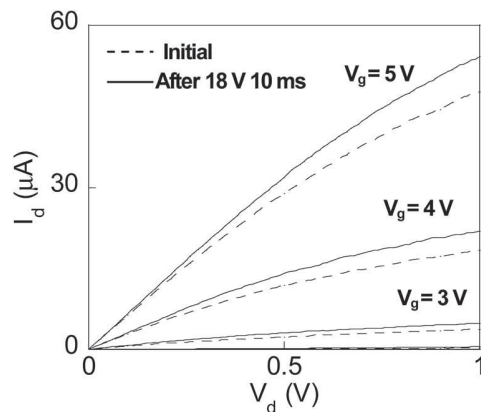


FIG. 4. Drain current (I_d)-drain voltage (V_d) characteristics as a parameter of gate voltage (V_g) before (broken line) and after (solid line) positive bias V_g application (18 V, 10 ms).

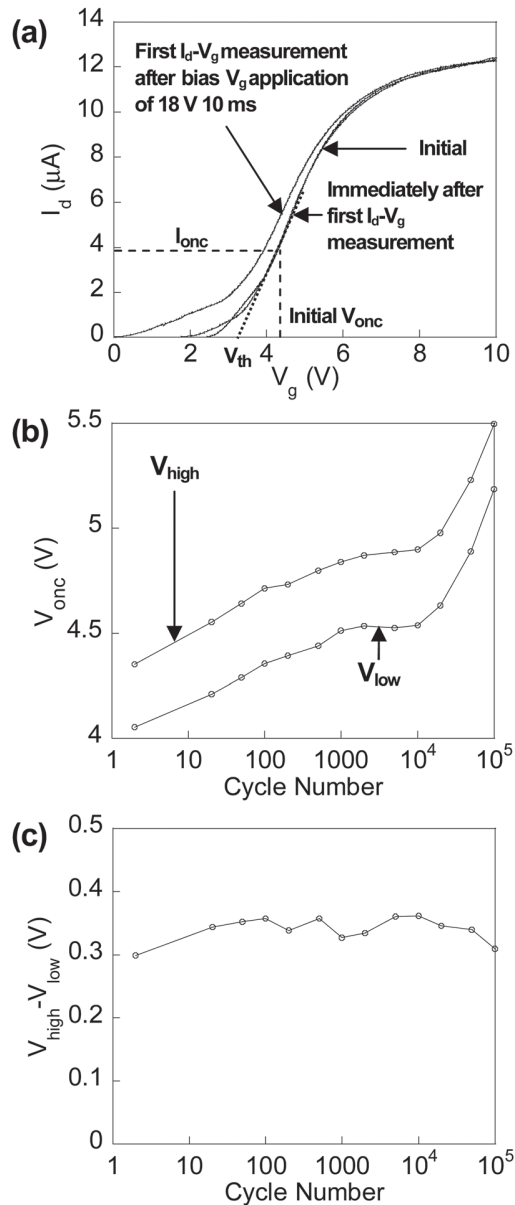


FIG. 5. (a) Initial drain current (I_d)-gate voltage (V_g) characteristics and those of the first measurement after a positive bias V_g application (18 V, 10 ms). Immediately after the first I_d - V_g measurement, the I_d - V_g characteristics were measured again. The dotted line illustrates the linearly extrapolated threshold voltage (V_{th}) at the initial I_d - V_g characteristics. Broken lines also indicate I_{onc} (defined as I_d at the V_{th} plus 1.0 V) and V_{onc} (defined as V_g at I_{onc}) at the initial I_d - V_g characteristics. (b) Endurance characteristics of the tunnel and lower gate oxides. V_{low} is V_{onc} for the measurement after the positive bias V_g application (18 V, 10 ms) and V_{high} is V_{onc} for the measurement before the positive bias V_g application. The measurement of V_{low} and V_{high} was carried out at 2, 20, 50, 100, 200, 500, 1000, 2000, 5000, 10 000, 20 000, 50 000, and 100 000 cycles. (c) Dependence of the voltage difference between V_{high} and V_{low} in (b) on the cycle number. The device used in the measurement in Fig. 5 is different from that in Fig. 3.

As described later, this increase is mainly caused by electrons that get trapped in the lower gate oxide during the positive bias V_g applications. However, as shown in Fig. 5(c), the voltage difference between V_{high} and V_{low} remained approximately constant (almost the initial value of 0.3 V) even after 10^5 cycles of electron ejection and injection.

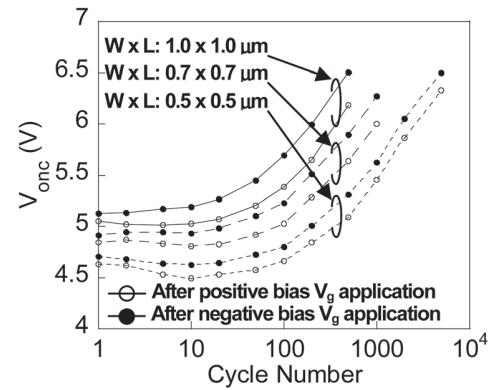


FIG. 6. Dependence of oxide breakdown characteristics on the channel size. V_{low} and V_{high} are the V_{ox} after positive and negative bias V_g applications, respectively. V_{low} and V_{high} were measured at 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000, 2000, and 5000 cycles.

Figure 6 shows the dependence of the oxide breakdown characteristics on the size of the channel region. The widths (W) \times lengths (L) of the channels were $0.5 \mu\text{m} \times 0.5 \mu\text{m}$, $0.7 \mu\text{m} \times 0.7 \mu\text{m}$, and $1.0 \mu\text{m} \times 1.0 \mu\text{m}$. The initial V_{ox} values were 4.7, 5.0, and 5.3 V for the respective devices. The applied values of positive and negative biases were 15.4 and -6.0 V, 15.7 and -5.7 V, and 16.0 and -5.6 V, respectively. To make the number of transferred electrons almost the same in injection and ejection, the positive and negative biases were set so that the absolute values of the difference between the initial V_{ox} and the positive bias were equal to that between the initial V_{ox} and the negative bias. In the endurance measurement, a large $I_{g\text{leak}}$ eventually flowed from the gate electrode to the source/drain electrodes through the channels. This indicates that breakdown occurred in both the tunnel and lower gate oxides.

Figure 7 shows the dependence on the channel size of the cycle number at which both the tunnel and lower gate oxides broke down. The figure shows results for a device with a channel size of $0.8 \mu\text{m} \times 0.8 \mu\text{m}$ in addition to those from Fig. 6. Breakdown occurred at 7753, 2273, 809, and 605 cycles for the respective channel sizes of $0.5 \mu\text{m} \times 0.5 \mu\text{m}$, $0.7 \mu\text{m} \times 0.7 \mu\text{m}$, $0.8 \mu\text{m} \times 0.8 \mu\text{m}$, and $1.0 \mu\text{m} \times 1.0 \mu\text{m}$. This clearly shows that the cycle number at oxide breakdown

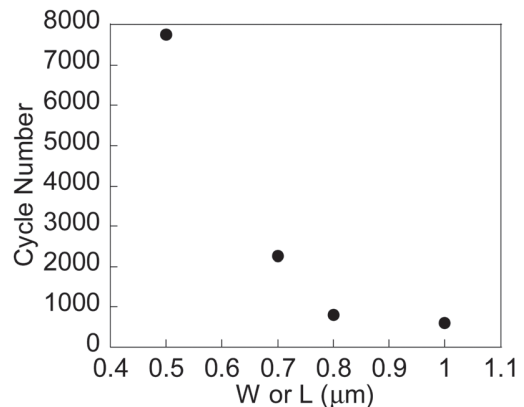


FIG. 7. Dependence on the channel size of the cycle number at which the breakdown of both the tunnel and lower gate oxides occurred.

increases as the channel size decreases. Therefore, the smaller the channel is, the less often breakdown occurs, meaning that electron traps randomly form in the oxide.

Figure 8 shows the dependence on the channel size of the voltage difference between V_{onc} after a positive bias V_g application (V_{low}) and after a subsequent negative bias V_g application (V_{high}). Here too, the results for a device with a channel size of $0.8 \mu\text{m} \times 0.8 \mu\text{m}$ have been added. The value of $V_{high}-V_{low}$ remained approximately constant after 100 cycles, especially for two devices ($W \times L$: $0.5 \mu\text{m} \times 0.5 \mu\text{m}$ and $1.0 \mu\text{m} \times 1.0 \mu\text{m}$). The tendency in the other two devices was to be constant, as well. Therefore, the difference between the number of injected and ejected electrons after 100 cycles is considered to be slight.

V. DISCUSSION

The endurance characteristics of the devices were analyzed in order to clarify the breakdown mechanism of the tunnel and lower gate oxides. Figure 9 shows the breakdown characteristics of the gate oxide for two different devices fabricated on the same wafer as a function of the number of cycles of positive and negative bias V_g applications. Here, the negative bias was applied in order for high-speed injection of electrons into the charge trap layer. The two devices had the same structure and channel size ($L = 0.5 \mu\text{m}$, $W = 0.5 \mu\text{m}$) and thicknesses of tunnel and lower gate oxides. One device, which is referred to as “type A” hereafter, kept an approximately constant $V_{high}-V_{low}$ during the positive and negative bias V_g applications above 5000 cycles [Fig. 9(a)]. After 5000 cycles, oxide breakdown was accompanied by a large I_{leak} , indicating both tunnel and lower gate oxides broke down. In contrast, the other device, which is referred to as “type B” hereafter, $V_{high}-V_{low}$ gradually decreased as the cycle number increased and this window eventually closed [Fig. 9(b)]. The difference between V_{high} and V_{low} at around 10^4 cycles was 0.02 V, whereas the initial value was 0.12 V. I_{leak} was still smaller than the noise level at around 10^4 cycles. As described below, the tunnel gate oxide would have broken down immediately after the lower gate oxide broke down, leading to a large I_{leak} . Therefore, we considered that the

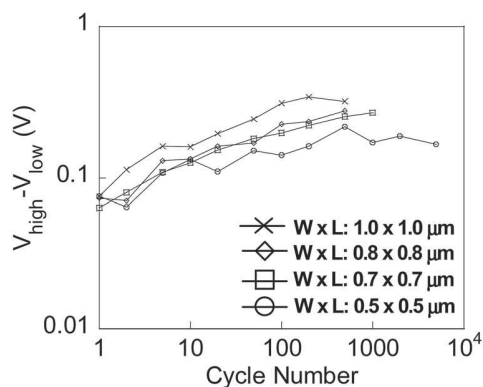


Fig. 8. Dependence of the voltage difference between V_{high} and V_{low} on the cycle number for different channel sizes.

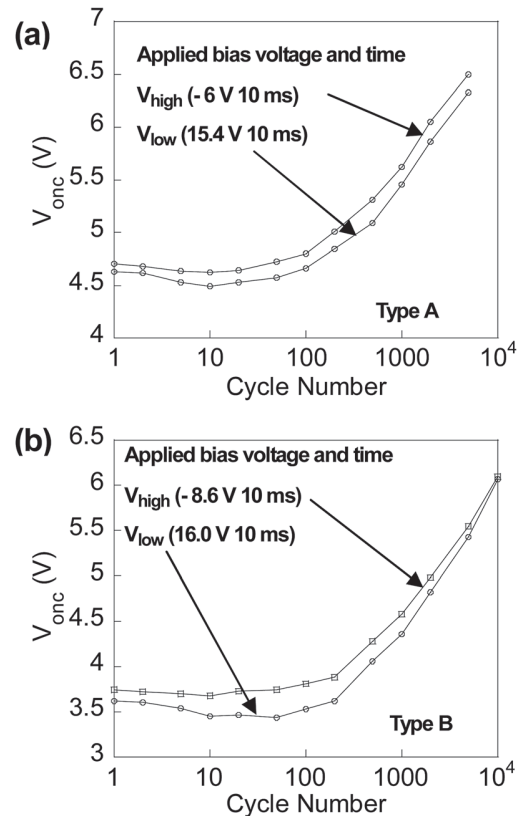


Fig. 9. Two types of oxide breakdown [(a) type A and (b) type B] as a function of cycles of positive and negative bias V_g applications. (a) V_{low} and V_{high} are V_{onc} after positive (15.4 V) and negative (-6.0 V) bias V_g applications (10 ms). (b) V_{low} and V_{high} are, respectively, V_{onc} after positive (16.0 V) and negative (-8.6 V) bias V_g applications (10 ms). V_{low} and V_{high} were measured at 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000, 2000, and 5000 cycles.

lower gate oxide did not break down in this device. Note that the number of fabricated devices showing type-A characteristics was much larger than those showing type-B characteristics.

We consider that these two types of device have different oxide deterioration and breakdown mechanisms. In particular, the lower gate oxide must have broken down in the type-A devices since a large leakage gate current was detected. Once that occurred, the whole V_g was applied only to the remaining thin tunnel gate oxide and the electric field in the tunnel gate oxide increased to an extremely high value. Were we to assume that oxide breakdown does not occur in the tunnel oxide, the electric field would be 64 MV/cm. This value is much larger than the breakdown fields of typical oxides, around 10 MV/cm,¹³ and this means the tunnel gate oxide must have immediately broken down after the lower gate oxide did.

The thickness of the lower gate oxide was 10 nm, and it is well known that a percolation model accurately explains how oxides with such thicknesses break down.^{14–16} In reference to our results, application of the bias V_g caused a high electric field at the lower gate oxide and this generated electron traps. According to the percolation model, the electron traps that were generated in the lower gate oxide became

connected and acted as a conductive path from the charge trap layer to the channel. This led to breakdown of the lower gate oxide. Indeed, the increase in V_{high} and V_{low} after 10 cycles in the type-A device [Fig. 9(a)] is considered to have been caused by an increase in the trapped electrons in traps generated in the lower gate oxide.

On the other hand, lower gate oxide did not break down in the type-B devices. The gradual closing of the window between V_{high} and V_{low} with the cycle number can be explained as follows.¹⁷ Besides the increase in the trapped electrons in the lower gate oxide, the number of trapped electrons in the tunnel gate oxide gradually increased with the cycle number. These trapped electrons decreased the tunnel efficiency through the tunnel gate oxide during the negative and positive V_g biases. This led to a decrease in the number of electrons injected into the charge trap layer through the tunnel gate oxide during a negative bias, which resulted in a decrease in V_{high} . Similarly, the number of electrons ejected from the charge trap layer decreased as a result of the decrease in tunnel efficiency through the tunnel gate oxide during the positive bias V_g application. This helped to increase V_{low} . The decrease in V_{high} and increase in V_{low} caused the window of $V_{high}-V_{low}$ to close. Note that besides the above effects on V_{th} , there was also a base increase in V_{th} caused by the trapped electrons in the lower gate oxide, as described before in the discussion of type A. Combining this base increase effect with the above effect, we can see that the rise in V_{low} becomes much sharper compared with the rise in V_{high} [see Fig. 9(b)]. The window did not close when the breakdown of the lower gate oxide occurred before 10^4 cycles. Therefore, the window closing would have appeared in most of the devices if the lower gate oxide did not break down after 10^4 cycles.

Next, we will discuss the reason for the dependence of the breakdown characteristics on the channel size by using the percolation model.¹⁴⁻¹⁶ As shown in Fig. 7, the smaller the channel is, the less often breakdown occurs. The breakdown of the lower gate oxide is caused by the generated electron traps connecting the charge trap layer and the channel. Only one such conductive path is enough to cause the lower gate oxide to break down. Since the electron traps are distributed randomly in the lower gate oxide, the probability of forming one conductive path becomes larger as the channel size increases. Therefore, the endurance characteristics of the oxide improve as the channel size decreases.

Then, let us discuss the way to increase the operation speed of our device. It took somewhat long for the fabricated device to return to the off-current state from a high voltage, as shown in Fig. 5(a). Strictly speaking, use of the proposed device in logic applications would necessitate a quicker recovery to the off-current state. The conventional CMOS logic used in personal computers operates at a few gigahertz, and advanced logic applications require the operation frequencies over 10 GHz, which corresponds to an operation time of 0.1 ns. In the fabricated device, one of the ways to make the operation time as short as 0.1 ns is to reduce T_{ox} to 0.5 nm. According to an extrapolation from the experimental

data of electron tunneling injection and ejection,¹⁸ the operation time is as short as 0.1 ns when T_{ox} is 0.5 nm with bias V_g application. Though such a thin T_{ox} seems very difficult to realize, it will soon be possible by utilizing techniques such as atomic layer deposition (ALD).^{3,19-22} Indeed, a thin (physical thickness of 0.5 nm) Si nitride was successfully deposited on a Si substrate by ALD as a barrier layer of ZrO_2 gate dielectrics.^{21,22} Even if such an ultimate deposition technique is not used, our device would still have applications that normally operate at a lower frequency. In particular, the relatively long characteristic time would not necessarily be a problem in ultralow power applications for watches, health care devices, and passive radio frequency integrated circuit tags.

Furthermore, the decrease in the thickness of the tunnel gate oxide will lead to a decrease in the power-delay product (PDP) due to the shorter electron ejection time from the charge trap layer. As mentioned before, the operation time of our device can be reduced to about 0.1 ns for a thickness of 0.5 nm. With a drain current of 10 μA and drain voltage of 0.1 V, the PDP becomes about 0.1 fJ, which is smaller than that of present logic operations whose order ranges from fJ to pJ.

With continued device scaling, fluctuations in V_{th} may become relatively large and be a problem for proper logic operations. One solution is to use the verify process which makes the V_{th} shift uniform among devices. In flash memory, it takes about 200 μs for a whole program/verify process. For logic circuits, the operation time seems to be too long; however, the verify process can be used in some ultralow power logic applications, such as watches whose typical operation time is 1 s. From the viewpoint of fabrication, on the other hand, separating the charge trap layer to multiple parts or increasing the number of floating gates is one idea to make V_{th} shift uniform. Even if the size of each trap layer varies, the size distribution in the trap layers will be similar, and this will reduce the V_{th} variation among the devices. Another idea is to reduce the thickness variation of the tunnel oxide by using the techniques such as ALD. Such a reduction would enable the variation in the number of injected and ejected electrons to be reduced, which makes V_{th} shift uniform among devices. If we can reduce the variation of V_{th} shift among devices to some extent by using the above fabrication processes, we can further reduce the whole time for the verify process.

Finally, it should be noted that while our devices showed the self-adjustment of V_{th} due to the relatively thick tunnel oxide in this study, the positive bias V_g necessary for the electron ejection from the charge trap layer can be much decreased by reducing the thickness of the tunnel gate oxide. In this case, since electron ejection leads to a sharp rise in I_d when the device is switched from the off-state to the on-state, small S -factors can appear. When the device is switched from the on-state to the off-state, on the other hand, electrons are injected to the charge trap layer, which also results in a decrease in the S -factor. This would enable us to increase the on-current without increasing the off-current for ultralow power operation.

VI. CONCLUSION

We devised a functional gate MOSFET and demonstrated its operating principle, which enables the on-current to be increased without increasing the off-current for ultralow power operation. Prototype devices were fabricated, and the systematic study of the fundamental device characteristics necessary for ultralow power operation were demonstrated putting emphasis on the device reliability. A negative V_{th} shift was caused by electron ejection, and a positive V_{th} shift was caused by electron injection. The measured endurance characteristics of the tunnel and lower gate oxides indicated that oxide breakdown did not occur until 10^5 electron ejection-and-injection cycles when only a positive bias V_g was applied. Endurance characteristics showed that the number of cycles to breakdown increases as the channel size decreases. We also found two different oxide breakdown characteristics. In one type, both the lower and tunnel gate oxides broke down. In the other, the window between V_{high} and V_{low} closed before oxide breakdown occurred. We explained these oxide breakdown mechanisms with a percolation model. Since a smaller channel greatly improves the endurance characteristics and the decrease in T_{ox} leads to high-operation speed, the scaling down of the device will open the way to the development of CMOS logic applications for it in the sub-32 nm technology node.

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Functional gate metal-oxide-semiconductor field-effect transistors using tunnel injection/ejection of trap charges enabling self-adjustable threshold voltage for ultralow power operation

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Metal-oxide-semiconductor field-effect transistors (MOSFETs) with a functional gate, which enables self-adjustment of threshold voltage (V_{th}), were proposed for ultralow power operation and fabricated with conventional complementary metal-oxide-semiconductor (CMOS) technology. In the on-current state of fabricated nMOSFETs, electron ejection from the charge trap layer by direct tunneling makes V_{th} low and increases on-current further. In the off-current state, electron injection into the charge trap layer makes V_{th} high and suppresses subthreshold leakage current. Although the characteristic time of electron transfer of the functional gate from on-current state to off-current state is fairly long, the logic mode operating principle has been verified with the experimental device. Reduction of tunnel oxide thickness (T_{ox}) will reduce the time, which will lead to the practical use of the proposed device for CMOS logic application. © 2011 American Institute of Physics. [doi:10.1063/1.3549178]

Extensive effort has been devoted to scaling metal-oxide-semiconductor field-effect transistors (MOSFETs) for low power consumption large-scale integrated circuits (LSIs).¹ The introduction of high- k gate dielectrics has also been intensively studied for power reduction.^{2,3} However, the fundamental difficulty in decreasing threshold voltage (V_{th}) and/or S -factors in scaling MOSFETs limits the further reduction of power supply voltage. S denotes subthreshold swing. As power (P) is proportional to V_{DD}^2 (V_{DD} is the power supply voltage), a lowering of V_{th} by 0.1 V with keeping the gate overdrive voltage same corresponds to a 20% reduction of power consumption in advanced complementary metal-oxide-semiconductor (CMOS) LSIs. However, a lowering in V_{th} generally accompanies an increase in the off-current. To avoid this increase, it is necessary to achieve a small S -factor or to adjust V_{th} to a high value in the off-current state and to a low value in the on-current state. To date, tunnel field-effect transistors (FETs),⁴ ferroelectric-gate FETs,^{5,6} and suspended-gate MOSFETs^{7,8} have been proposed and have attracted significant interest to achieve S -factors lower than 60 mV/sec. However, there are still issues with these potential devices for process cost and compatibility with already existing CMOS fabrication technology. In this study, we propose a MOSFET with a functional gate that enables V_{th} self-adjustment for low power operation. We fabricated a prototype device with conventional CMOS fabrication technology and showed the fundamental device characteristics necessary for low power logic operation.

A schematic diagram is shown in Fig. 1. The structure of the proposed MOSFET resembled that of the conventional floating gate memory. Only the difference was that a thin tunnel gate SiO_2 existed between the floating gate and top gate electrode for the proposed functional gate. Electrons

transferred between the floating gate and the top gate electrode in the proposed device. The thicknesses of the tunnel gate oxide (T_{ox}) and lower gate oxide were 1.2 and 10 nm, respectively. The poly-Si floating gate was formed for the charge trap layer. The thickness of the floating gate was 70 nm. The device fabrication process was similar to that of the floating gate memory previously reported^{9–11} with a slight modification. Silicon-on-insulator wafer was used and electron beam lithography was utilized to define the floating gate and channel. The thickness of the Si channel was 60 nm. The channel width and length were 1.0 and 18 μm , respec-

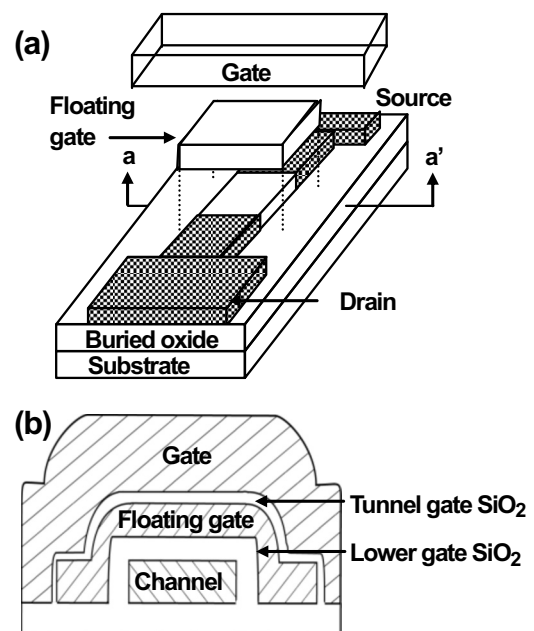


FIG. 1. (a) Schematics of fabricated functional gate MOSFET. The shaded regions are heavily As^+ implanted. (b) Cross-sectional view along a-a' line in (a). Thicknesses of the tunnel gate oxide, lower gate oxide, and Si channel were 1.2, 10, and 60 nm, respectively.

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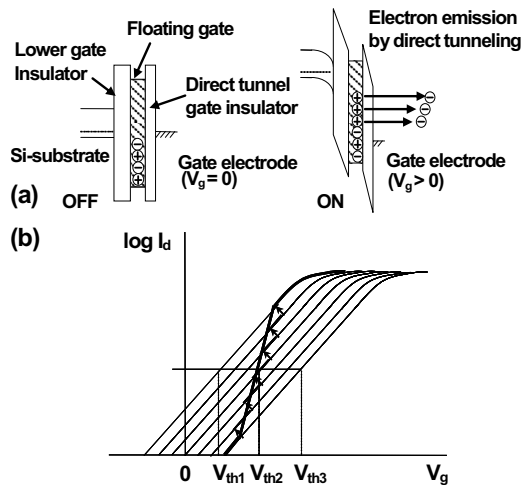


FIG. 2. (a) Band diagram of functional gate structure for the proposed MOSFET in the off-current and on-current states. (b) Operating principle of self-adjustment of threshold voltage for ultralow power operation of the proposed functional gate MOSFET.

tively. After defining the channel area and forming the lower gate oxide, an amorphous Si film was deposited for the floating gate. Then, the resist line was formed parallel to the channel, and dry etching was carried out to define the width of the floating gate. The width of the floating gate was $1.6 \mu\text{m}$, which was slightly larger than that of the channel. While the tunnel gate oxide was formed, the amorphous Si of the floating gate changed to poly-Si. After that, a poly-Si film was deposited for the top gate electrode. The resist line was formed perpendicularly across the channel, and the dry etching was stopped upon reaching the lower gate oxide. The length of the floating gate and the top gate electrode were the same ($1.0 \mu\text{m}$) using this self-aligned etching process.

The band diagram of the functional gate structure and operation principle of the proposed nMOSFET are shown in Figs. 2(a) and 2(b), respectively. Since the gate voltage (V_g) was sufficiently low in the off-current state, no electron transfer occurred from the floating gate to the top gate electrode [Fig. 2(a)], keeping V_{th} high [V_{th3} in Fig. 2(b)]. On the other hand, V_g was large enough in the on-current state, and electrons transferred from the floating gate to the top gate electrode [Fig. 2(a)]. This led to additional lowering of the surface potential of the channel, making V_{th} low [V_{th1} in Fig. 2(b)] and increasing the on-current further. In this way, the proposed MOSFET could increase the on-current without increasing the off-current, leading to ultralow power operation.

Figure 3 shows the dependence of drain current (I_d)- V_g characteristics on bias V_g application. In Fig. 3(a), V_{th} was measured after the positive bias V_g (which varied from 1 to 10 V with a voltage step of 1 V) was applied to the gate electrode for 60 s. While V_{th} shift did not occur until the positive bias voltage was 7 V, V_{th} shifted to the negative side above 8 V, which was the opposite direction to that of conventional floating gate memory, showing that the trapped electrons were indeed ejected from the floating gate. Owing to the relatively large T_{ox} , V_g over 8 V was necessary to eject electrons from the floating gate by direct tunneling for 60 s of V_g application time. When V_{th} was defined as V_g at an I_d of 10^{-7} A, the value of V_{th} shift was -0.15 , -0.53 , and -1.06 V for a V_g application of 8, 9, and 10 V, respectively. Here, V_{th} was returned to around the initial V_{th} value by the

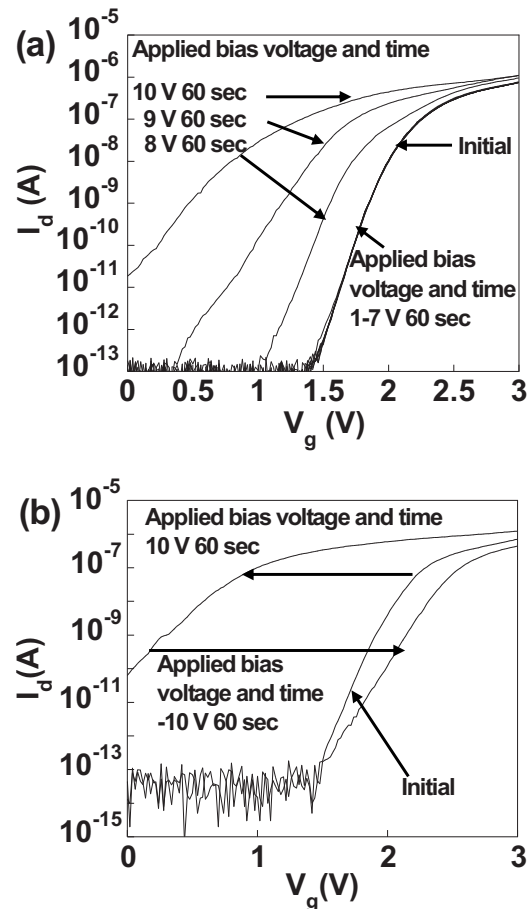


FIG. 3. Bias voltage dependence of I_d - V_g characteristics. $V_d=0.1$ V. (a) After 60 s of application of positive bias V_g (1–10 V with 1 V steps) was applied, I_d - V_g curve was obtained. (b) I_d - V_g characteristics after positive bias V_g application (10 V, 60 s) and subsequent negative bias V_g application (-10 V, 60 s).

procedure described later before each V_g application and the V_{th} shift were measured from the returned value. For these V_g applications, effective voltage of 0.9–1.1 V is estimated to be applied to the tunnel gate oxide. Therefore, self-adjustment of V_{th} , which increased the on-current, was realized keeping the off-current low. By the application of negative V_g , V_{th} returned to close to the initial V_{th} value [Fig. 3(b)]. After the positive V_g application of 10 V for 60 s, the subsequent negative V_g application of -10 V for 60 s made V_{th} shift to the positive side, showing the electron injection into the floating gate. The direction of the V_{th} shift was also opposite to that of conventional floating gate memory.

Figure 4 shows I_d -drain voltage (V_d) characteristics after the positive and negative bias voltage applications. Typical I_d - V_d characteristics such as clear saturation were obtained after both the positive and negative V_g applications. Consistent with the results in Fig. 3, the on-current is indeed larger after the positive V_g application of 10 V for 60 s than after the subsequent negative V_g application of -10 V for 60 s.

Figure 5 shows the dependence of I_d - V_g characteristics on time after the application of positive V_g . After the V_g application, it was seen that V_{th} slowly returned to the initial V_{th} value; electron injection into the floating gate occurred slowly. The characteristic time was found to be over an hour. Although it took a long time to become off-current state, the off-current became sufficiently low. Strictly speaking, to use the proposed device for logic applications, quick recovery

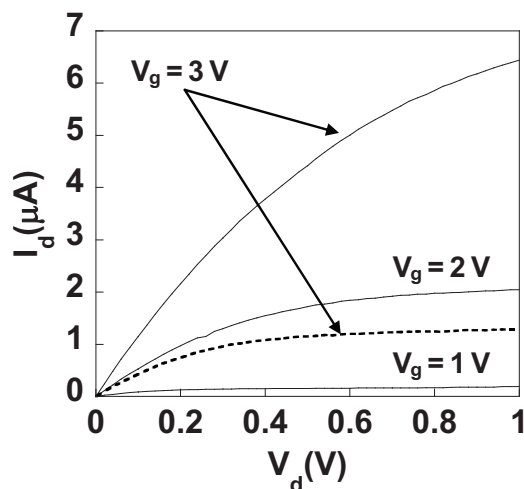


FIG. 4. I_d - V_d characteristics as a parameter of V_g after the positive bias V_g application (10 V, 60 s) (solid line) and subsequent negative bias V_g application (-10 V, 60 s) (broken line).

to the off-current state is necessary when V_g returns to 0 V from a high voltage. The way to make the time as short as 0.1 ns is to reduce T_{ox} to 0.5 nm. According to an extrapolation from the experimental data of electron tunneling injection/ejection,¹² the time becomes as short as 0.1 ns when T_{ox} is reduced to 0.5 nm. Though it looks very difficult to realize such a thin T_{ox} , it will be possible utilizing techniques such as an atomic layer deposition (ALD).^{3,13-16} Indeed, a thin (physical thickness of 0.5 nm) Si nitride was successfully deposited on a Si substrate by ALD as a barrier layer of ZrO_2 gate dielectrics.^{15,16} For a thin tunnel oxide with $T_{ox} = 0.5$ nm, tunnel current density is simulated to be about 10^5 A/cm² at a gate voltage of 0.5 V for an n^+ -gate/p-Si nMOSFET.¹⁷ Using the tunnel current density, the injected/ejected charge amount ΔQ to/from the floatin gate is 10^{-5} C/cm² during a switching time of 0.1 ns. Then, the threshold voltage shift ΔV_{th} accompanied with the charge injection/ejection is calculated to be 1.4 V from $\Delta V_{th} = \Delta Q/C$. Here, the capacitance C between the upper gate and

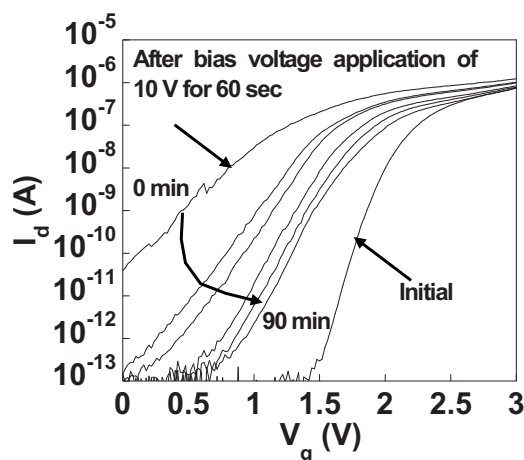


FIG. 5. Time dependence of I_d - V_g characteristics after the positive bias V_g application (10 V, 60 s). I_d - V_g curves were measured at 0, 5, 10, 30, 60, and 90 min after the V_g application. $V_d = 0.1$ V.

the floatin gate is 6.9×10^{-6} F/cm² since the upper gate oxide is the tunnel gate oxide ($T_{ox} = 0.5$ nm) for the device in this study. Therefore, sufficient ΔV_{th} is considered to be obtained at $T_{ox} = 0.5$ nm for the ultralow power logic application. It should be noted that, as far as for the ultralow power logic applications to such as watches, health care devices, or passive radio frequency integrated circuit tags, the relatively long characteristic time may be allowable and T_{ox} can be much larger than 0.5 nm.

Finally, it should be noted that for reliability enhancement, making the floatin gates plural may be effective. Separating the trap charge layers into plural ones could effectively avoid the V_{th} shift caused by the production of a leakage pass as can be seen in the case of floatin dot memory.¹⁸⁻²⁰

In summary, the operating principle of functional gate MOSFETs, which enables V_{th} self-adjustment for ultralow power operation, has been proposed. A prototype device was fabricated, and fundamental device characteristics necessary for the self-adjustment of V_{th} have been demonstrated. Reduction of T_{ox} will make the characteristic time of electron transfer short and will open the way to CMOS logic applications.

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- (1) “Development of Biosensor Using Si Nanowire Transistor”
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Development of Biosensor Using Si Nanowire Transistor

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In the field of medical science, to establish the method of highly sensitive and selective detection of a protein is strongly needed. Si nanowire (SiNW) field effect transistor has been used in a highly sensitive detection of their charge; however, it is very difficult to distinguish the target substance from a mixture. To overcome this problem, sticking an antibody on the gate insulator surface through silicon-binding-protein (SBP) [1] will be a key technology. This will make possible to detect the charge density change due to the specific binding of the antibody to the antigen. For that goal we have first tried to detect the SBP's charge. Here we report the charge of SBP could be successfully detected in real time.

We have fabricated a SiNW ion-sensitive field-effect transistor (ISFET) on silicon-on-insulator (SOI) wafer by the top-down process. We have made SiNW from top-Si layer by using an electron-cyclotron-resonance etcher. Scanning electron microscopy (SEM) image of SiNW in the fabricated ISFET and schematic diagram for the measurement setup of electrical characteristics are shown in Fig. 1 (a) and (b), respectively. The overall dimension of the SiNW is approximately $5\ \mu\text{m} \times 80\ \text{nm} \times 17\ \text{nm}$ (length \times width \times height). The ISFET is of the n-MOSFET. The gate insulator is composed of two layers: a lower one is thermally grown SiO_2 and an upper one is CVD-grown Si_3N_4 .

Figure 2 shows the source-drain current (I_{ds}) versus gate voltage (V_{g}) characteristics of the ISFET at three buffer solutions (10

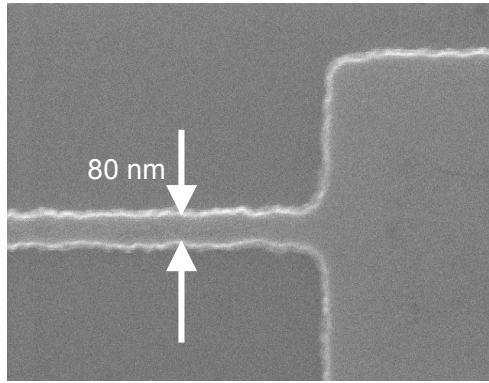
mM tetraborate, pH 9, 50 mM phosphate, pH 7 and 50 mM phthalate, pH 4) on the channel. The source-drain voltage (V_{ds}) was fixed at 100 mV. It should be noted that the threshold voltage shift is about 60 mV/pH, which is in good agreement with that theoretically obtained by Nernst equation. Figure 3 displays the I_{ds} modulation at the V_{ds} of 100 mV and the V_{g} of 800 mV by varying the buffer solutions on the channel. The source-drain conduction increases (decreases) as the acidity of the solution increases (decreases).

We have also monitored the response of our device to the charge of SBP. We have prepared the SBP solution (1×10^{-2} mg SBP in 20 μl of 1 mM tetraborate buffer, pH 9), in which the SBP has about +30 charges. Figure 4 shows time dependence of the I_{ds} at V_{ds} of 100 mV and at V_{g} of 400 mV. While the SBP is flowing on the channel, charges of the SBP increase the gate bias. The result indicated that the SBP are smaller in size than the Debye length and SBP's charge are successfully monitored by the SiNW ISFET.

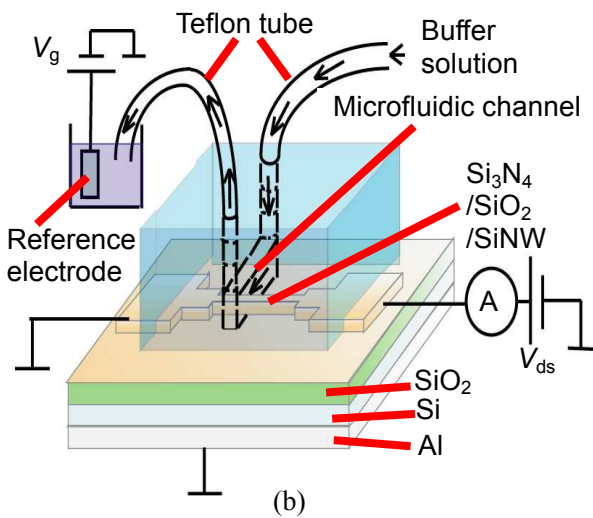
In summary, we have fabricated the SiNW ISFET on SOI wafer by the top-down process. By using the ISFET, we have obtained threshold voltage shift of about 60mV/pH which is consistent with that theoretically estimated by the Nernst equation. We have also performed the real-time detection of the SBP. The ability to monitor the SBP flowing on the channel area and to sense the charge of SBP has been confirmed.

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(a)



(b)

Fig.1. (a) SEM image of Si nanowire and (b) schematic diagram for measurement setup of electrical characteristics.

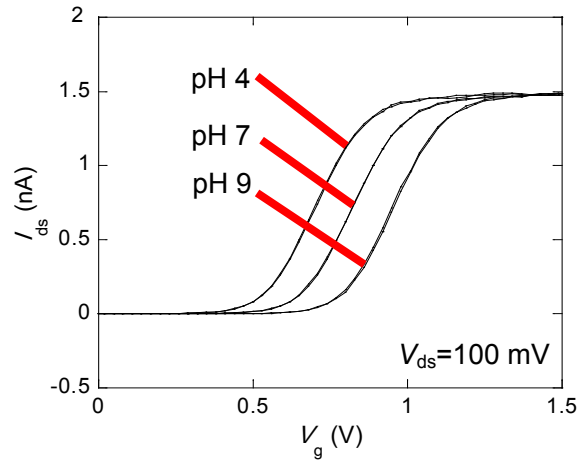


Fig.2. I_{ds} - V_g characteristics of SiNW transistor at pH 4, pH 7 and pH 9. The thicknesses of the SiO₂ layer and the Si₃N₄ layer are 15 nm and 42 nm, respectively.

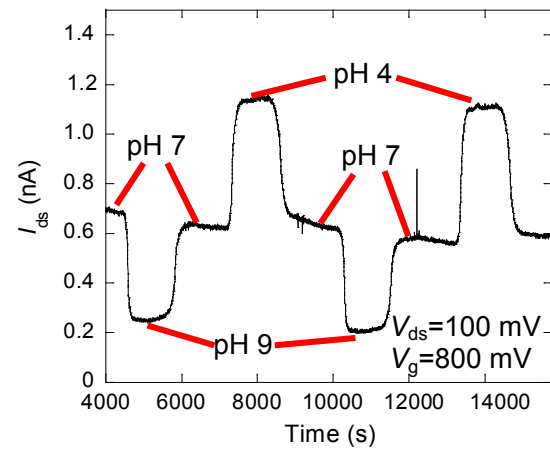


Fig.3. pH-response characteristics of the SiNW transistor. The thicknesses of the SiO₂ layer and the Si₃N₄ layer are 15 nm and 42 nm, respectively.

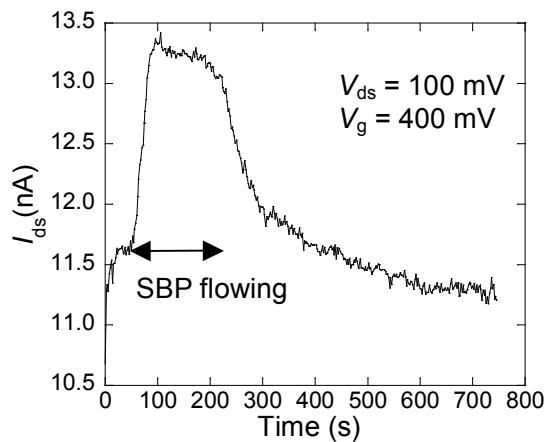


Fig.4. SBP-response characteristics of the SiNW transistor. The thicknesses of the SiO₂ layer and the Si₃N₄ layer are 2 nm and 15 nm, respectively.