

広島大学学位請求論文

Development and Verification of
Compact Model for NBTI (Negative
Bias Temperature Instability) Effect
Observed in p-MOSFET

p-MOSFETにおけるNBTI (Negative
Bias Temperature Instability)
効果のモデル開発

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1. 主論文

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〔p-MOSFETにおけるNBTI (Negative Bias Temperature Instability) 効果のモデル開発〕

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主論文

博士論文

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Abstract

In the next 10 years, the dimension of semiconductor devices will scale towards 10nm. Consequently the reliability of ULSI circuits and systems faces enlarged challenges due to the introduction of the new materials and non-classical structures. Especially, the negative bias temperature instability (NBTI) effect is one of the most important reliability concerns since it deteriorates the drive-capability of the p-MOSFETs by degrading threshold voltage, drain current, transconductance, resulting in output delay. An accurate predictive NBTI effect model is required for protective circuit design and reduction of design tolerances to save the layout area. At present, numerous NBTI predictive model based on different physical theories have been developed, including hydrogen reaction-diffusion theory, hole-trapping theory, energy profile based theory and so on. However, an effective NBTI model must accurately predict the following features: 1) Long term degradation under DC stress conditions. 2) AC degradation with various frequencies and duty cycles. 3) The recovery characteristic in short term and long term regions. 4) Temperature dependence.

In this thesis, a predictive NBTI compact model has been developed. New physics based explanations are introduced to explain all reliability phenomena including those observed most recently. The main achievements of this thesis are as follows:

- 1) A basic reaction-limited-diffusion NBTI model is developed using the hydrogen reaction-diffusion theory. The reaction process of Si-H bond is investigated in detail and described by using a dynamic balance equation. The forward reaction rate is supposed to decrease with increased stress time due to the accumulation of H atoms within the gate oxide. Combined with the hole-trapping mechanism, the NBTI model shows good agreement with the measured data under DC and AC conditions.
- 2) Measurement results obtained under ultra fast measurement conditions indicate that the original hydrogen-diffusion theory has a limitation in describing the high frequency NBTI effect. Hole-trapping theory becomes a widely accepted

explanation for logarithmic time dependence of the threshold voltage degradation (ΔV_{th}). The reaction of silicon bonds are supposed to generate interface states under the stress conditions. By recalculating the gate oxide field influenced by the interface states, the logarithmic time dependence of ΔV_{th} is physically derived. Combined with the hole-trapping theory, the newly developed NBTI model is effective in describing the degradation under various conditions, including stress bias, stress/recovery processes different technologies and materials, frequency dependence and duty cycles changes.

- 3) In a real circuit, p-MOSFETs are operated with not only the gate bias (V_{gs}), but also the applied drain bias (V_{ds}). Therefore, the degradation induced by V_{ds} is unable to be neglected due to the evidently enhanced channel lateral electrical field. In this thesis we developed hot carrier enhanced NBTI model and implemented this predictive model into HiSIM. Combining both NBTI and hot carrier effect model, the threshold voltage degradation under any operation conditions can be predicted.
- 4) In order to carry out the prediction of circuit performances, the developed NBTI model is implemented into the compact MOSFET model HiSIM. The degradation of the threshold voltage is equivalent to a shift of the flat-band voltage, which directly impacts the electric field, potential and current. Therefore the performance degradation of the circuit is able to be simulated.

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Chapter 1 Introduction

1.1 Recent Development of Microelectronics Technology

In the past 40 years, the continuously rapid development of semiconductor industry has greatly promoted the human society progress. The efforts on innovation and competition of scaling the device dimensions and increase the integration density of the layout were never stopped since the birth of the first integrated circuit. According to the International Technology Roadmap for Semiconductors (ITRS'2012) [1.1], as shown in Fig. 1.1.1, the half pitch dimension of DRAM and flash memory has been scaled to 30nm, and tends to beyond 10nm till the year 2025. Since the dimension is scaled down beyond 45nm, the short channel effect (SCE) is observed to be more seriously impact the device performance. To suppress the SCE, new structures and materials are introduced, e.g. ultra-thin gate oxide, high channel dopant, high-K gate dielectrics, multi-gate MOSFET and so on.

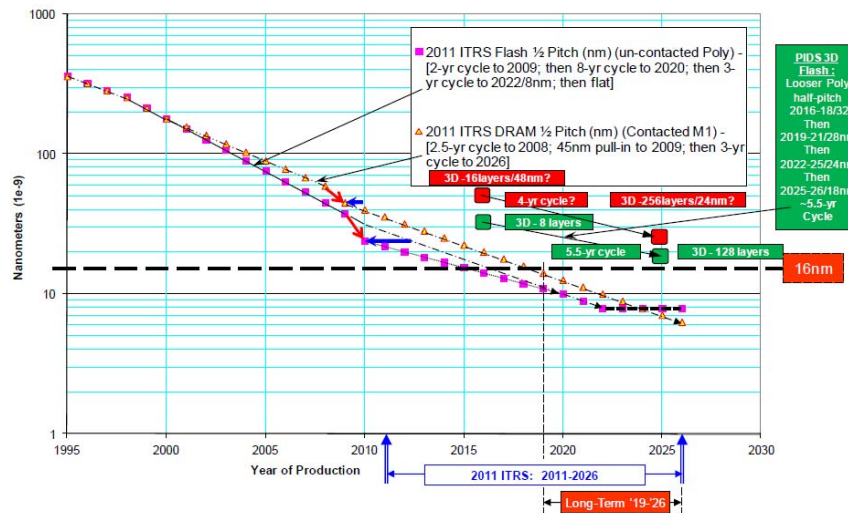


Fig. 1.1.1. 2012 ITRS-DRAM and flash memory half pitch trends

The dimension of the semiconductor device is scaling down following Moore's Law and approaching to its limitation. Since the year 2010, an "equivalent scaling" is proposed, which provided a possibility to extend Moore's Law beyond its limitation. As shown in Fig. 1.1.2, high-K gate dielectrics and high mobility channel materials are introduced to the MOSFET manufacture. Moreover, FinFET fabricated based on bulk and SOI wafers have been

commercialized by leadership companies. However, although the development of new device structure and materials attracted considerable attention of semiconductor industry, the traditional CMOS device is incapable to be completely replaced. CMOS circuits still act as cores no matter whether on chip-level or on package-level. Therefore, detail investigation on device physics and simulation methodologies is necessary for CMOS design optimization.

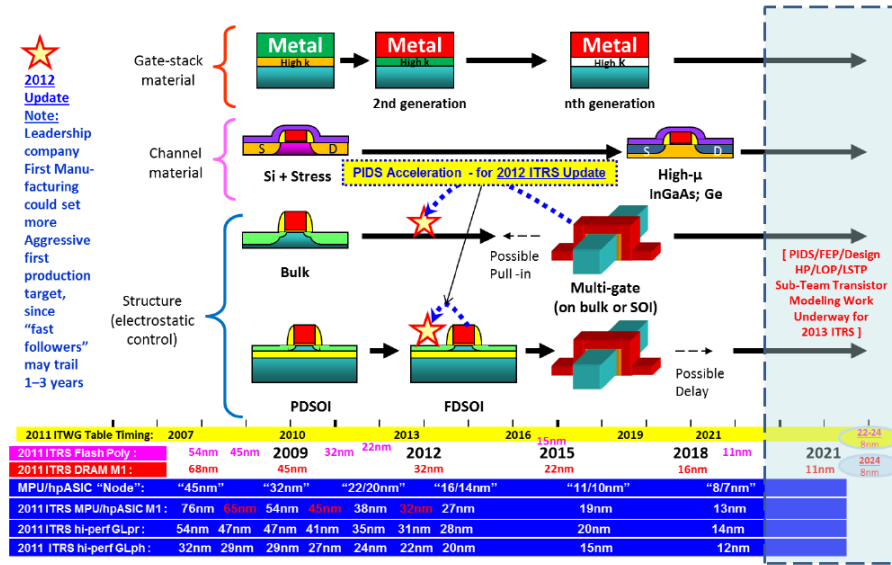


Fig. 1.1.2. 2011 ITRS “Equivalent Scaling” process technology timing, ORTC MPU high-performance ASIC half pitch and gate length trends and timing, and industry “nodes”

1.2 Negative Bias Temperature Instability (NBTI) Effect

The aggressive scaling down of the MOSFETs results in an increase of the internal electric field both in the channel and the gate oxide. Moreover, in order to reduce the gate leakage and enhance the carrier mobility, high-K dielectrics, strain engineering and high mobility channel materials are applied. However, they are accompanied with inevitable high concentration of defects within the materials as well as at the interface [1.2-1.9]. It has been reported that, when the gate of p-MOSFET is negatively biased (Fig. 1.2.1), the NBTI effect is caused by positive charged oxide traps and interface states. This increases the delay time of the circuit critical path with increased operation time, which reduces the circuit speed and lifetime. In long term operation conditions, p-MOSFETs suffer from continuous stress and recovery cycle, and 20% delay increase during 5-10 years' operation is expected [1.10]. In order to avoid the impact of degradation to logic functions, the design tolerance may increase to 30% under the worst case. However, the increased design tolerance inevitably results in higher complexity and area of the circuit design. Therefore, analyzing the NBTI sensitive part

of the circuit and developing accurate predictive model is the key for approach cost saving and optimization design.

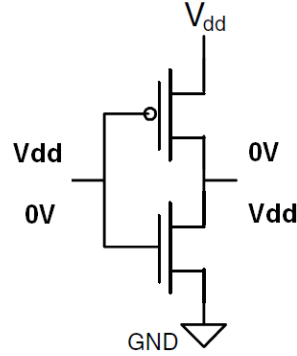


Fig. 1.2.1. Bias conditions during circuit operation of a CMOS inverter. With input is 0V, output is high and the p-MOS device (top) is under uniform negative gate bias, which causes NBTI degradation.

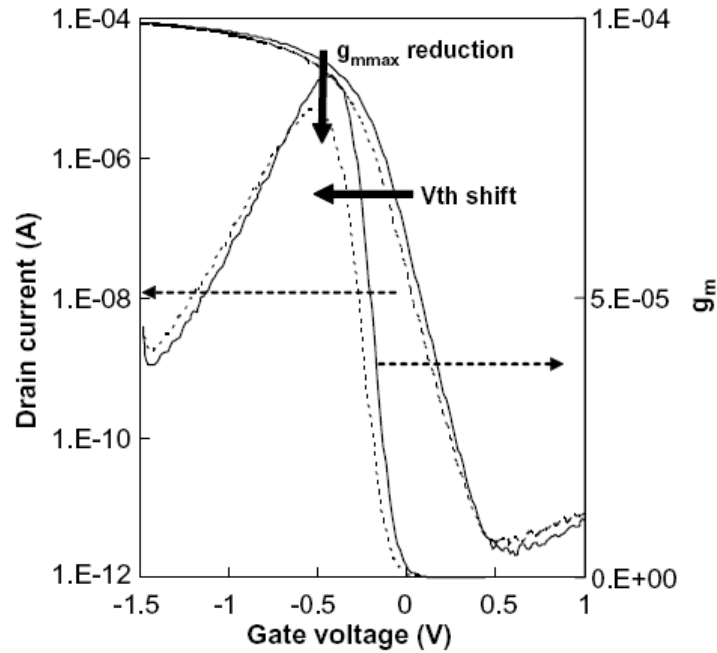


Fig. 1.2.2. The degradation of I_d-V_g and g_m-V_g curves of p-MOSFET before and after 10000s NBTI stress. The gate oxide thickness is 2nm, and temperature is 125°C. Solid and dashed lines indicate the characteristic before and after stress, respectively.

During circuit operations, carriers have great opportunity to be captured by such defects or generate new traps under high electric field. The charged traps are quite possible to degrade the threshold voltage, subthreshold slope, current, and transconductance. The degradation of current characteristics induced by the NBTI effect is shown in Fig. 1.2.2 [1.11]. After 10000s stress, the threshold voltage, On-state current and transconductance exhibit evident

degradation. The above degradation deteriorates the lifetime and speed of the circuit and system [1.12], and even leads to logic failure. For the standard 6-T SRAM case as an example (Fig. 1.2.3), the static noise margin (SNM) is degraded up to 10% after 10 years' usage.

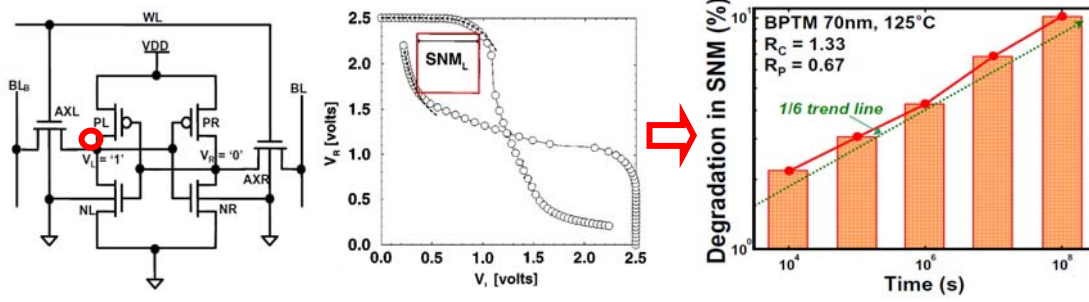


Fig. 1.2.3. The impact of NBTI effect to static noise margin (SNM) in 6-T SRAM. The degradation is up to 10% after 10 years' usage.

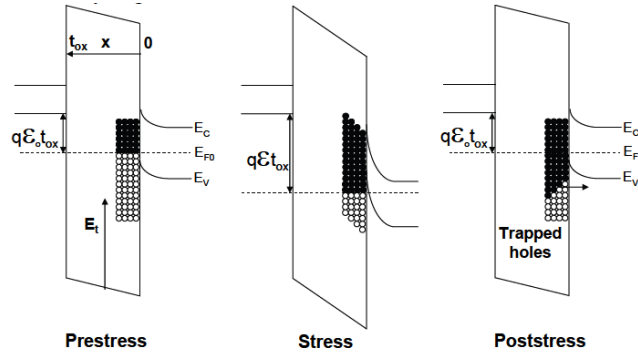


Fig. 1.2.4. Hole trapping diagram. (a) prestress: traps are empty (b) during stress: traps are filled by holes and (c) poststress: trapped holes tunnel out. [1.14].

Under the conditions of negative bias and high temperature, the NBTI effect is induced by high density of interface-state and gate oxide traps [1.13]. As shown in Fig. 1.2.4, under negative bias, the interface states and oxide traps are positively charge and results in the threshold voltage shift. When the stress is removed, part of the trapped charges is released and reenters into the substrate [1.14]. The threshold voltage shift is determined by the generation of interface states and oxide traps.

$$\Delta V_{th} = q(\Delta N_{it} + \Delta N_f) / C_{ox} \quad (1-2-1)$$

Here q is electron charge, C_{ox} is gate oxide capacitance, ΔN_{it} and ΔN_f are densities of generated interface states and gate oxide traps, respectively.

Another widely acceptable explanation for NBTI degradation is based on the theory of Si-H bond dissociation and hydrogen diffusion. As illustrated in Fig. 1.2.5, high density of Si-H bond is located at the Si/SiO₂ interface. When negative bias is applied to the gate, holes are injected from substrate into the gate oxide, and possibly break down the Si-H bonds. Hydrogen atoms diffuse towards the gate contact and leave Si dangling bonds behind, which act as interface states and degrade the threshold voltage [1.15]. After stress is removed, part of the hydrogen atoms diffuses back to repair the dangling bonds, leading to the recovery of threshold voltage.

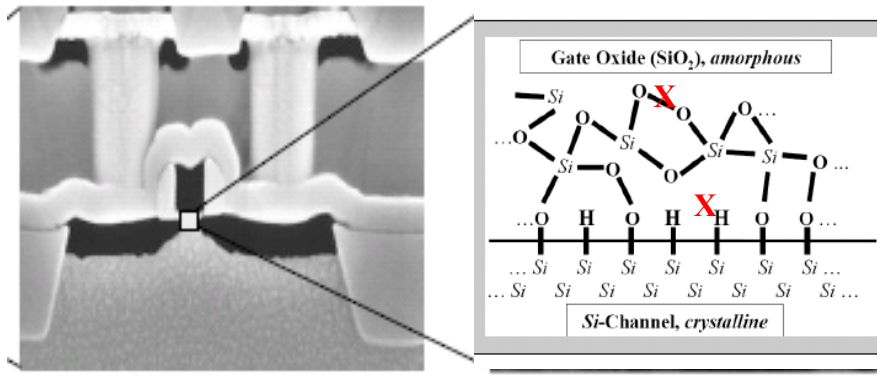


Fig. 1.2.5. NBTI effect explanation based on Si-H reaction and hydrogen diffusion theory.

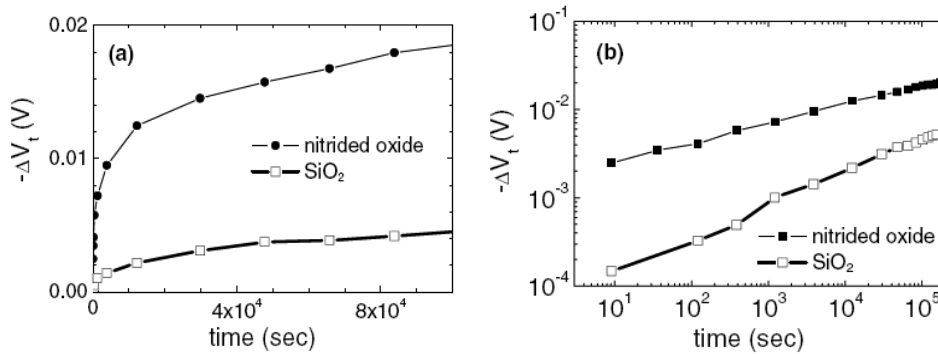


Fig. 1.2.6. Typical threshold voltage shift characteristics with increased stress time. The introduction of nitrogen into the gate oxide results in larger NBTI degradation compared to the traditional SiO₂ dielectrics. (a) Linear scale. (b) Semi-log scale.

Typical results of ΔV_{th} as a function of the stress time are shown in Fig. 1.2.6. Large device is used to avoid the impact from structure limitation as well as statistic process fluctuation. The relationship between ΔV_{th} and stress time typically follows a power-law relationship (e.g. $\Delta V_{th} \sim t^{0.2}$). With the introduction of new gate dielectric material, NBTI

induced ΔV_{th} shows different mechanisms. The nitride gate dielectric is observed featuring enhanced NBTI degradation [1.16] when compared to the traditional SiO_2 gate oxide.

The stress bias dependence of the threshold voltage degradation (ΔV_{th}) is shown in Fig. 1.2.7. ΔV_{th} increases with the increased stress bias and approximately exhibits a “power-law” time dependence under high stress bias conditions. However, in the low stress bias condition, ΔV_{th} shows different characteristics in short term and long term region. This phenomenon is mainly due to the hole-trapping/detrapping mechanism, which will be discussed in detail later.

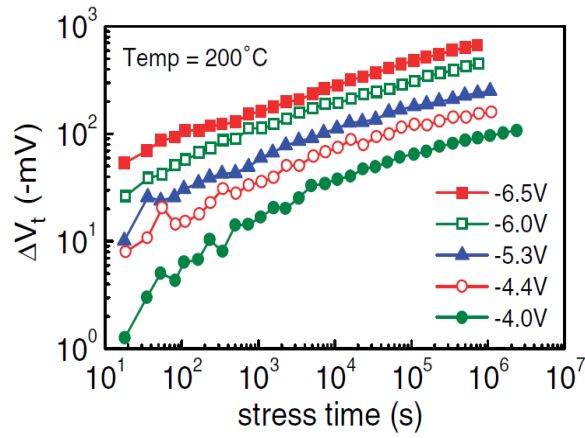


Fig. 1.2.7. ΔV_{th} versus stress time for various stress biases on p-MOSFET with 6.7nm gate oxide [1.13].

The NBTI effect is widely accepted closely correlated to the vertical gate oxide electric field. Even under the same stress bias condition, the increase of oxide thickness results in weakened oxide field and results in less V_{th} degradation, as shown in Fig. 1.2.8.

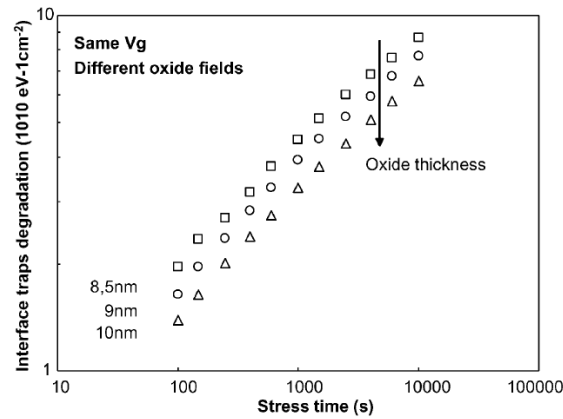


Fig. 1.2.8. Interface traps creation for p-MOSFETs after 10,000 s of stress for three different oxide thicknesses under similar gate voltage [1.17].

The temperature dependence is validated in Fig. 1.2.9. With fixed stress bias, the interface traps density shows more seriously increase with temperature elevated from 50°C to 200°C. This enhanced degradation is supposed as due to the increased active energy of the interface states as well as the existing traps.

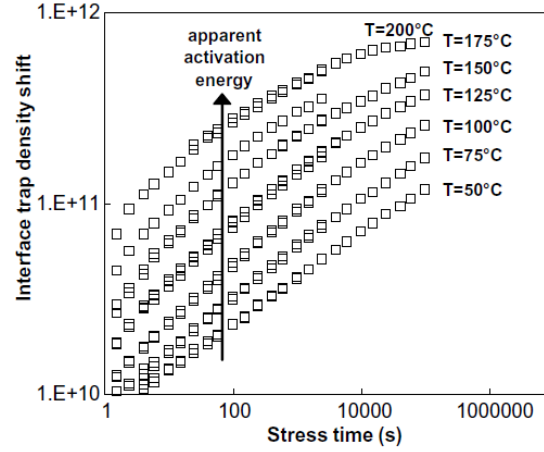


Fig. 1.2.9. Interface traps density shift under constant stress bias with temperature ranging from 50°C to 200°C. [1.17]

The ΔV_{th} under static and dynamic stress conditions are compared in Fig. 1.2.10. It is obvious that the dynamic NBTI effect induces less degradation. This is because of the essential recovery behavior of the NBTI effect once the stress bias is removed. With the increased frequency, the V_{th} degradation is reduced and even stays at relative stable level, as shown in Fig. 1.2.11.

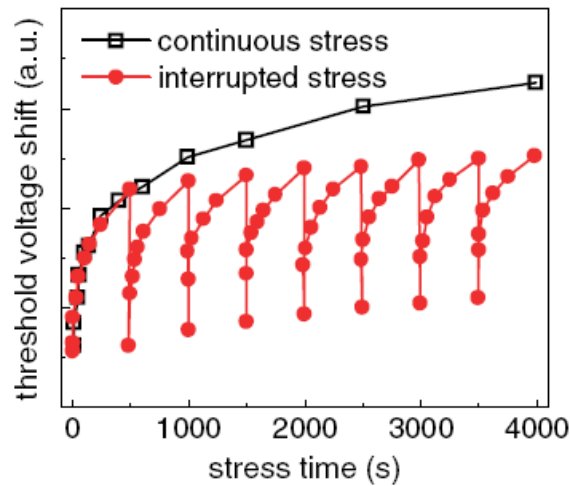


Fig. 1.2.10. V_{th} degradation under static ($V_g=-2.5V$) and dynamic (with recovery bias of $V_g=1.5V$) in p-MOSFET with 2nm SiON dielectrics. [1.13]

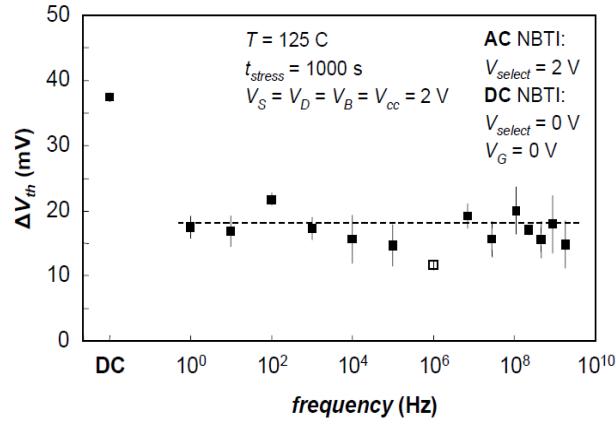


Fig. 1.2.11. V_{th} shift due to AC NBTI stress is observed independent of frequency over the range of 1Hz to 2GHz. [1.18]

The ΔV_{th} resulting from AC NBTI stress at 10kHz is extracted after 1000s stress duration, as shown in Fig. 1.2.12. A monotonic increase is observed with increased duty cycle due to the continuously increased stress time during each cycle. Especially, when duty cycle reaches 100%, the device is stressed under the worst case of DC condition.

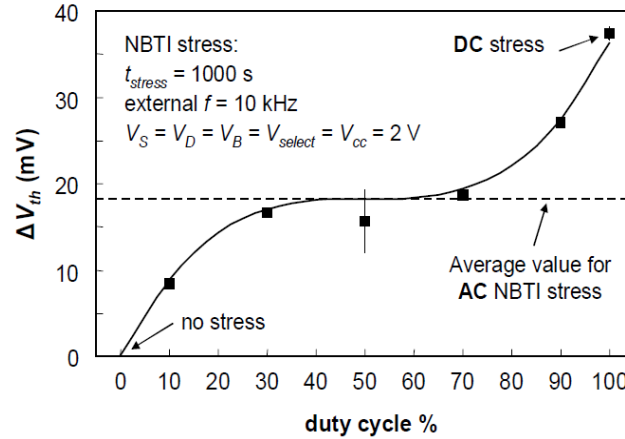


Fig. 1.2.12. ΔV_{th} resulting from AC NBTI at 10kHz with varying duty cycle. [1.18]

1.3 Purpose of This Research

The purpose of this study is developing a NBTI predictive model validated under any stress and temperature conditions. Besides of figuring out the physical mechanisms behind the NBTI degradation, the practicality of the compact predictive model is also highly concerned. The novel proposals to approach the purpose are as follows:

1. Developed NBTI model with the improved reaction-diffusion (RD) theory. The traditional RD theory assumes that the hydrogen diffusion in the gate oxide is the fundamental reason of the threshold voltage degradation under negative gate bias. In this thesis, the procedure of Si-H bond reaction is investigated in detail, and modeled using a logarithmic time dependent equation, which is physically derived from the classical reaction equation.
2. However, the assumption of hydrogen diffusion is still open for discuss, the hole-trapping/detrapping theory attracts close attention recently. In this thesis, the NBTI model is improved by combining the reaction of silicon bonds at the interface with the hole-trapping in the gate oxide. Based on the observation of the experimental results, the short term degradation is dominated by hole-trapping mechanism, while the long term degradation is induced by interface state generation.
3. In the real circuit, the drain of p-MOSFET is usually biased at the applied voltage. In order to ensure the NBTI model applicable under any practical operation conditions, the drain bias dependent hot carrier effect model coupling with NBTI model is developed. With the increased drain bias, the threshold voltage shift firstly decreases in the low drain bias region due to the weakened NBTI effect, and then increases in the high drain bias region due the enhanced hot carrier effect.
4. Temperature is the other significant factor responsible for p-MOSFET degradation. During the operation, the circumstance temperature may elevate to several hundred degree C. The result of NBTI predictive model without considering the temperature dependence may lead to 50% deviation from the real situation. Therefore, this thesis considers the temperature as another component of the developed NBTI model. The temperature dependence of all the model parameters is consistent with the experimental results reported previously.
5. The NBTI model is implemented into the advanced compact MOSFET model HiSIM for circuit simulation. The output-delay of inverter, ring oscillator, NAND, NOR, SRAM after certain time operation is simulated.

1.4 Organization of This Thesis

Chapter 1 makes a simple overview of the background of semiconductor development at present and in the future. NBTI effect is highlighted as one of the most significant reliability issues in today's IC design and manufacture. Then the motivation and organization of this thesis is introduced.

Chapter 2 gives an overview of the NBTI predictive model during the recently passed 10 years, with investigation of the superiority and the drawback in predicting the NBTI degradation under various conditions of bias and process.

Chapter 3 improves reaction-diffusion NBTI by considering the diffusion mechanism of Si-H bond at the Si/SiO₂ interface as well as the diffusion process in the poly-Si gate. The threshold voltage (V_{th}) degradation due to the Si-H bond reaction is modeled by solving the original reaction equation, and the reverse reaction component (recovery) is included consistently in the reaction process.

Chapter 4 develops a compact NBTI model describing the interface state generation and hole-trapping mechanisms. High accuracy of the developed NBTI model is validated by comparing with the measured data under various conditions of stress bias, time duration, technology and material, frequency and duty cycle. In order to make the NBTI model suitable for the simulation of real circuit, the impacts of drain bias and temperature are introduced. All the results show good agreement with the measurement data, and provide great possibility for predicting the degradation of real circuit during long time usage.

Chapter 5 shows the implementation of the NBTI model into the compact MOSFET model HiSIM for circuit simulation. In this chapter, the developed NBTI model is implemented into compact device model HiSIM. The degradation of the threshold voltage is equivalent to the shift of flat-band voltage, which directly impacts the electric field, potential and current. Therefore the performance degradation of the circuit is able to be simulated.

Chapter 6 concludes the thesis and makes prospects of the future work.

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Chapter 2 Overview of Existing NBTI Model

2.1 Introduction

At present, numerous NBTI predictive models based on different concepts have been developed, including the hydrogen reaction-diffusion theory, hole-trapping theory and the energy transfer based theory. However, none of them are able to balance both the consistency of the theory as well as the practical application. An efficient NBTI model must be able to accurately predict the following features: 1) Long term degradation under DC stress conditions. 2) AC degradation with various frequencies and duty cycle. 3) The recovery characteristic in short term and long term regions. 4) Temperature dependence. In the following part, the significant published NBTI predictive models, such as the reaction-diffusion (RD) model, the hole-trapping model, the interface-state generation model and energy transfer hole-trapping model, are simply reviewed from principle, verification, advantage and drawback.

2.2 Classical Reaction-Diffusion Model

Principle of the reaction-diffusion (RD) model is simply described as follows: when a negative bias is applied to the gate of p-MOSFET, high density holes are injected into the gate oxide from the substrate. Holes with high energy possibly react with the Si-H bonds located at the Si/SiO₂ interface, generating a Si dangling bonds and hydrogen atoms. When the Si dangling bonds are occupied by holes, such positively charged states will act as interface-states and results in the threshold voltage shift (ΔV_{th}). At the same time, H atoms released from the Si-H bonds diffuse towards gate electrode [2.1]. The diffusion concentration determines the reaction rate of the Si-H bonds. The schematic view of Si-H bond reaction and hydrogen diffusion is shown in Fig. 2.2.1 (a). The generation of interface state is determined by both Si-H bond reaction rate (illustrated by line 1 and 2 in Fig. 2.2.1 (b)) and diffusion

distance (line 3 and 4 in Fig. 2.2.1(b)). “Triangle” distribution is the simplest approximation for H diffusion [2.2].

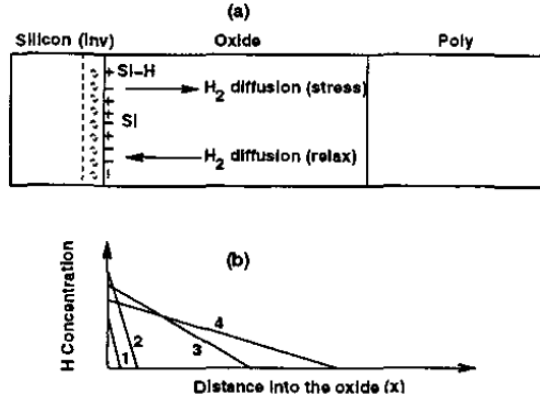


Fig. 2.2.1. (a) Schematic view of the RD model under stress and recovery conditions. (b) The hydrogen diffusion in the oxide is simply approximated as “triangle” distribution. The interface state generation is determined by both diffusion distance (3 and 4) and the reaction rate (1 and 2).

Eq. (2.2.1) describes the process of interface generation [2.1]. Here k_F and k_R are forward and reverse reaction rate respectively, N_0 is the initial trap density at the interface, N_H is the hydrogen concentration, and N_{it} is the interface-state density. Eq. (2.2.2) indicates the diffusion process, where D_H is the hydrogen atom diffusion constant.

$$\frac{dN_{it}}{dt} = k_F(N_0 - N_{it}) - k_R N_H N_{it} \quad (2.2.1)$$

$$\frac{dN_H}{dt} = -D_H \frac{d^2 N_H}{dx^2} \quad (2.2.2)$$

During the initial period of the reaction process, the generated interface-state density is much lower than the total density of Si-H bonds. Therefore, $dN_{it}/dt \approx 0$, and $N_0 \gg N_{it}$. Eq. (2.2.1) is simplified as

$$\frac{k_F N_0}{k_R N_{it}} = N_H \quad (2.2.3)$$

According to the diffusion equation (2.2.2), the hydrogen diffusion front x_D is solved as

$$x_D = \sqrt{D_H t} \quad (2.2.4)$$

As mentioned in Fig. 2.2.1(b), hydrogen atoms diffused into the gate oxide is supposed forming a triangle distribution. Thus the generated interface-state density is concentration is calculated by integrating the hydrogen within the gate oxide.

$$N_{it} = \frac{1}{2} N_{it0} x_D = \frac{1}{2} N_H x_D = \frac{1}{2} \frac{k_F N_0}{k_R N_{it}} \sqrt{D_H t} \quad (2.2.5)$$

The final expression of the interface-state density is

$$N_{it} = \left(\frac{1}{2} \frac{k_F N_0}{k_R} \right)^{1/2} (D_H t)^{1/4} \quad (2.2.6)$$

The traditional RD model was validated by comparing with the measurement result, as shown in Fig. 2.2.2. The V_{th} shifts following a power-law relationship with the stress time, and the time exponent is about 0.25~0.3, which is consistent with the model result [2.3, 2.4].

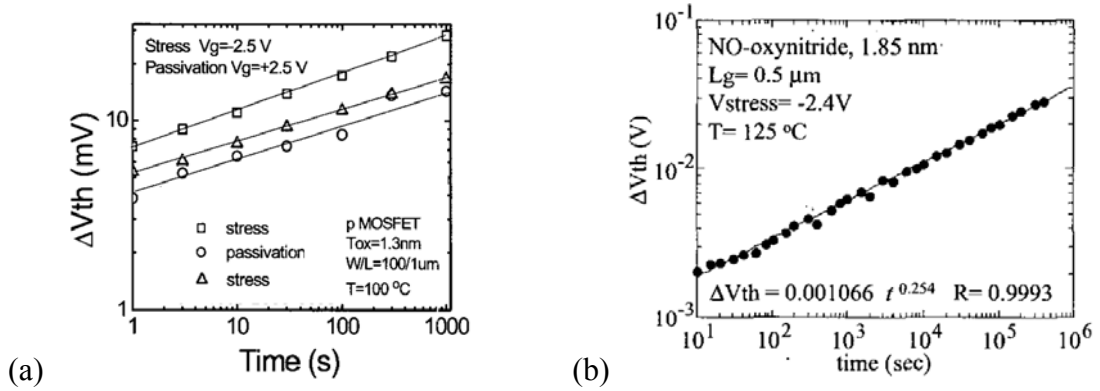


Fig. 2.2.2. Typical time dependence of NBTI. The log-log V_{th} shift versus stress time shows 0.25 time exponent. Data is from (a) [2.3] and (b) [2.4].

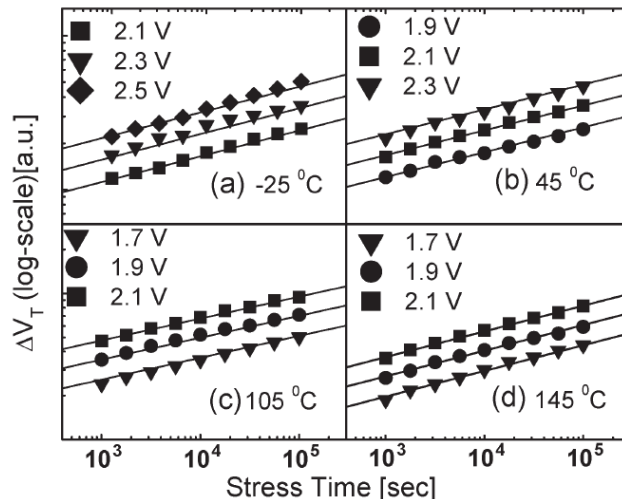


Fig. 2.2.3. (a–d) Fitting ΔV_T (measured by ultra-fast On-The-Fly technology) versus t (log–log scale) at different temperature and gate bias. Here, the slope $n = 0.15\text{--}0.16$ [2.7].

The time exponent of 1/4 is obtained based on numerous hypotheses, for example, slow reaction in the initial period, infinite gate oxide thickness and hydrogen atom diffusion process. However, soon after the proposed classical RD model, many measurement results obtained using advantage technologies showed that the time exponent featured 1/6 [2.5, 2.6], as shown in Fig. 2.2.3 [2.7].

Such phenomenon indicated that H atom diffusion is not the only element responsible for the NBTI degradation. In order to make a correct explanation to such phenomenon, A. Alam et al improved the classical RD model and assumed that part of the hydrogen atoms are possible to transfer into H₂ molecule during the diffusion procedure [2.8].

In Eq. (2.1.1), the H atom concentration is supposed as N_H . If the diffusion of H₂ is considered, the transfer between H₂ molecule and H atom is described as

$$N_H^{(0)} \propto \sqrt{N_{H_2}^{(0)}} \quad (2.1.7)$$

The diffusion process of H₂ molecule is

$$\frac{dN_{H_2}}{dt} = D_{H_2} \frac{d^2 N_{H_2}}{dy^2} \quad (2.1.8)$$

Similar to the classical RD model, the H₂ molecule diffusing in the gate oxide still follows the triangle distribution. Note that one H₂ molecule results in two Si dangling bonds, the interface state density (N_{IT}) is written as

$$N_{IT} = 2 \cdot \frac{1}{2} N_{H_2}^{(0)} \sqrt{D_{H_2} t} = N_{H_2}^{(0)} \sqrt{D_{H_2} t} \quad (2.1.9)$$

Substituting Eq. (2.1.3) into Eq. (2.1.7) and Eq. (2.1.9), the interface-state associated to the H₂ diffusion is derived as

$$N_{IT} \propto \left[\frac{k_F N_0}{k_R} \right]^{\frac{2}{3}} (D_{H_2} t)^{\frac{1}{6}} \quad (2.1.10)$$

The relationship between V_{th} shift and stress time is described using power-law equation in the RD model. The time exponent is insensitive to neither electric field nor temperature, but only determined by the diffusion series. If the diffusion series is H atom, the time

exponent is 1/4. Otherwise, the time exponent is 1/6

2.3 Improved RD Model Applied for Nano-Device

As mentioned in Section 2.2, the development of the RD model is based on numerous assumptions, such as slow generation of the interface state in the initial stage, infinite gate oxide thickness, and so on. Therefore, the classical RD model is insufficient in describing the NBTI effect in nanoscale MOSFETs with ultra thin gate oxide and special device structure. New mechanisms are needed to be considered and added to the RD model [2.9].

The schematic view of the silicon nanowire is shown in Fig.2.3.1. The nanowire diameter is 10nm, gate oxide thickness is 3.5nm with a TiN metal gate, gate length of the device is 427nm, and V_{th} is about 0.22V [2.10].

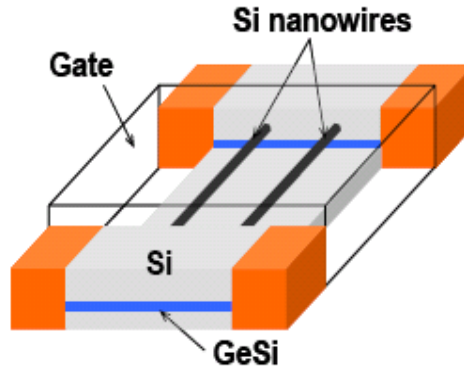


Fig. 2.3.1. The 3-D schematic view of the Twin Silicon Nanowire MOSFET.

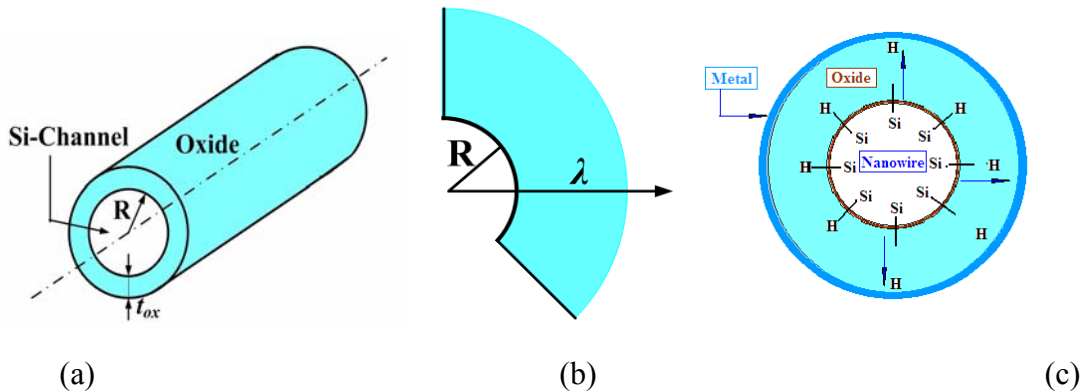


Fig. 2.3.2. (a) Cylindrical MOSFET with channel radius R ; the gate oxide surrounds the channel.(b) Hydrogen diffused from the Si-oxide interface along the radius of the nanowire, the diffusion constant is λ . (c) The schematic description of R-G model on the silicon nanowire cross-section.

In purpose of simplifying the theory derivation, the studied SNWFET is considered equivalent to a small scaled gate-surrounded MOSFET. Fig. 2.3.2(a) is a Cylindrical MOSFET with gate oxide surrounds the channel. R is channel radius and t_{ox} is the thickness of gate oxide. Fig. 2.3.2(b) shows a sketch view of Hydrogen diffuse from the Si-oxide interface along the radius of the nanowire, and the diffusion constant is λ . Hydrogen atoms are supposed diffusing along the radius to the gate dielectric, as shown in Fig. 2.3.2(c).

Based on the classical RD model from Eq. (2.1.1)-(2.1.4), hydrogen diffusion distance $\lambda(t) = \sqrt{D_H t}$, the density of H atom at the interface due to the diffusion expressed in cylindrical coordinates [2.11] is

$$N_{it}^0(t) = \frac{1}{2\pi RL} \int_R^{R+\lambda(t)} N_H \left(1 - \frac{r-R}{\sqrt{D_H t}} \right) 2\pi r L dr \quad (2.3.1)$$

Combining the integral result in Eq. (2.3.1) with (2.1.3) and supposing $\lambda(t) = \sqrt{D_H t}$, the concentration of H atom generated during stress process is

$$N_{it}^0(t) = \sqrt{\frac{k_f N_0 P}{R k_r}} \left(\frac{R \lambda(t)}{2} + \frac{\lambda(t)^2}{6} \right)^{\frac{1}{2}} \quad (2.3.2)$$

The inversion hole density P is dependent on the oxide electrical field (E_{ox}) [2.12] and the gate capacitance,

$$P = C_{ox} (V_{gs} - V_{th}) \quad (2.3.3)$$

Considering the special device structure of nanowire, the equivalent gate oxide thickness (t_{ox}) has the following relationship with the physical one (t_{ox0}) [2.13]

$$t_{ox} = R \ln \left(1 + \frac{t_{ox0}}{R} \right) \quad (2.3.4)$$

Considering that $\Delta V_{th} = q N_{it} / C_{ox}$, the degradation of threshold voltage (ΔV_{th}^0) derived by conventional R-D theory is obtained from Eqs. (2.3.2) and (2.3.3).

$$\Delta V_{th}^0(t) = \frac{q N_{it}^0(t)}{C_{ox}} = \frac{q t_{ox}}{\epsilon_{ox} \epsilon_0 \sqrt{R}} \left[\frac{1}{2^n} K^2 \left(\exp \frac{E_{ox}}{E_0} \right)^2 C_{ox} (V_{gs} - V_{th}) \right] \left(\frac{R \sqrt{Ct}}{2} + \frac{Ct}{6} \right)^{2n} \quad (2.3.5)$$

Here $n=1/4$ if the diffusing species was H, and $n=1/6$ if the diffusing species was H_2 ; C

was the diffusion constant dependent on the temperature and diffusing species; $T_0=10^{-8}s/nm^2$ was another constant; $E_a=0.49eV$ and $E_0=0.335V/nm$ for H_2 model; $E_a=0.12eV$ and $E_0=1.9\sim 2.0V/nm$ for H model [2.14]; $K=5.2\times 10^4$ was the field acceleration pre-factor; E_{ox} was the oxide electrical field; $R=5nm$ was the radius of the Si nanowire, other parameters contained their normal meaning. Noting that the diffusing species used here was H, so $n=1/4$, $E_a=0.12eV$, $E_0=2.0V/nm$ in this work.

Different from the assumption of the infinite oxide thickness, the H atoms diffusing into the gate oxide tends to saturate in the ultra thin gate oxide. The saturation rate R_{sat} is expressed as

$$\Delta V_{th}(t) = \frac{qN_{it_max}}{C_{ox}} \cdot R_{sat} = \frac{qt_{ox}}{\varepsilon_{ox}\varepsilon_0} \sqrt{\frac{k_f N_0}{Rk_r}} C_{ox} (V_{gs} - V_{th}) \left(\frac{R\lambda(t_1)}{2} + \frac{\lambda(t_1)^2}{6} \right)^{\frac{1}{2}} \cdot (1 - e^{-\frac{t}{\tau}}) \quad (2.3.6)$$

Here τ is the H atom capture time constant in the gate oxide.

A good agreement is obtained by comparing the modeling result with the measured data under stress bias of $V_{gs}=-2.4V$ and $-2.2V$, as shown in Fig. 2.3.3.

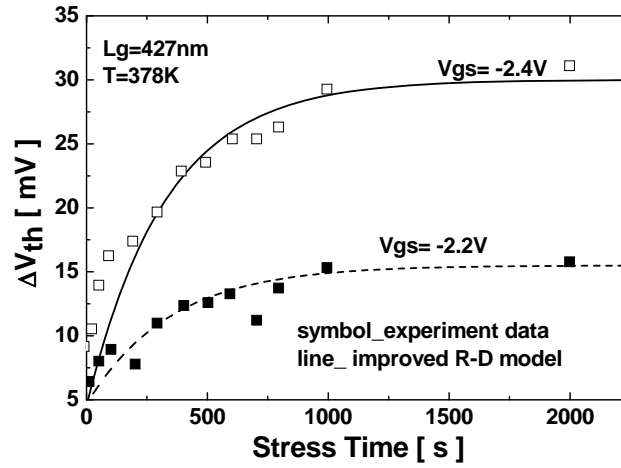


Fig. 2.3.3. Comparison between modeling result and the measured data under stress bias of $V_{gs}=-2.4V$ and $-2.2V$,

The recovery model is derived as an inverse process of the stress period. The ΔV_{th} during the recovery process is written as the difference between the maximum V_{th} shift (ΔV_{th_max}) and the recoverable ΔV_{th} (ΔV_{th}^R).

$$\begin{aligned}
 \Delta V_{th}^R(t) &= \Delta V_{th_max} - \Delta V_{th}^R \\
 &= \Delta V_{th_max} - \frac{qt_{ox}}{\epsilon_{ox}\epsilon_0} \sqrt{\frac{k_f N_0}{Rk_r}} C_{ox} (V_{gs} - V_{th}) \left(\frac{Rt_{ox}}{2} + \frac{t_{ox}^2}{6} \right)^{\frac{1}{2}} \cdot e^{-\frac{t-t_s}{\tau_r}}
 \end{aligned} \quad (2.3.7)$$

Here t_s is the stress time period, and τ_r is the time constant for H atoms released from the oxide traps. If the recovery model is developed based on the classical RD theory, the ΔV_{th} during the recovery process is derived as [2.15]

$$\begin{aligned}
 \Delta V_{th}^R(t) &= \frac{qN_{it}^0(t)}{C_{ox}} = \frac{q}{C_{ox}} (N_{it}^{str} - N_{it}^{rec}) \\
 &= \frac{qN_{it}^{str}}{C_{ox}} \left(1 - \frac{N_{it}^{rec}}{N_{it}^{str}} \right) = \frac{qN_{it}^{str}}{C_{ox}} \left[1 - \frac{\frac{R\sqrt{\xi D(t-t_1)}}{2} + \frac{\xi D(t-t_1)}{6}}{\frac{R\sqrt{Dt}}{2} + \frac{Dt}{6}} \right]
 \end{aligned} \quad (2.3.8)$$

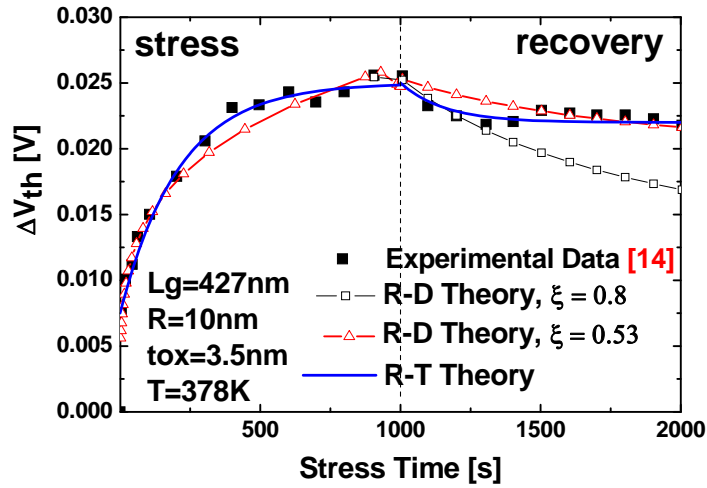


Fig. 2.3.4. Comparison of the experiment data (solid symbol) with both Standard RD model (open symbol) and improved RD model (line).

Fig. 2.3.4 compares the experimental data with both R-D model and newly developed model. It is obviously that, the improved model has evidently improved the quality and accuracy in matching with experimental data, especially in the recovery process. Such phenomenon indicates that the classical RD model is not sufficient for describing the NBTI degradation in nanoscale device. The limitation of the structure and hydrogen diffusion saturation effect should be considered in the predictive model.

2.4 Hole-Trapping/Detrapping Model

With the improvement of the measurement technology, the ΔV_{th} is demonstrated highly sensitive to the measurement delay due to the essential recovery characteristic of NBTI effect. The V_{th} exhibits distinct degradation characteristics for different measurement technologies, as shown in Fig. 2.4.1 [2.16]. The delay time of each technology is compared in Table. 2.4.1. The result shows that ΔV_t obtained with slow measurement technologies, the time dependence is approximately power-law function with time exponent of 1/6. However, the result obtained by fast measurement shows a much smaller time exponent around 0.07. Such result is inconsistent with the RD model even considering the transfer between H atom and H₂ molecule.

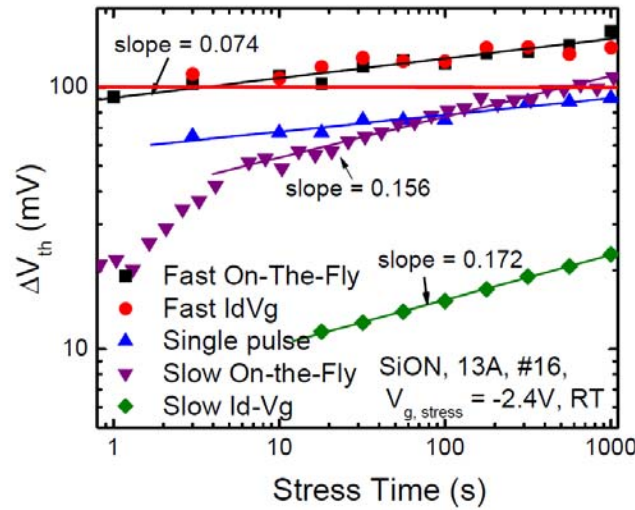


Fig. 2.4.1. ΔV_{th} measured with five different measurement technologies, which yield distinct NBTI results.

Table. 2.4.1. Summary of measurement technologies.

Method	Source of error	Effect on measured ΔV_{th}
Slow on-the-fly	Initial pre-stress I_d measurement ($V_g = V_{stress}$) is too slow, during which I_d degrades.	large under-estimation
Fast on-the-fly	Initial pre-stress I_d measurement (100-200 ns) induces small stress and thus small I_d degradation.	small under-estimation
Fast $I_d - V_g$	Small recovery after stress is removed, during the V_g sweep measurement (100-200 ns).	small under-estimation
Single pulse ΔI_d	Long settling time is required for good accuracy (< 1%), during which recovery occurs.	small-medium under-estimation

Except for the DC degradation measured by various technologies, AC NBTI degradation further demonstrates the drawback of the RD model. As shown in Fig. 2.4.2, the dynamic NBTI degradation is simulated using RD model. The maximum and minimum ΔV_{th} (ΔV_{th_max} and ΔV_{th_min}) generally merged together and became frequency independent after several stress/recovery cycles. However, this result is obviously inconsistent with the measurement results, as shown in Fig. 2.4.3. The differences of amplitude between ΔV_{th_max} and ΔV_{th_min} with various frequencies are evident distinguished and never merged together even after several stress/recovery cycles. Fig. 2.4.4 extracts the frequency dependence of ΔV_{th_max} and ΔV_{th_min} . The hole-trapping model exhibits a much higher accuracy than RD model in calculating the AC NBTI degradation.

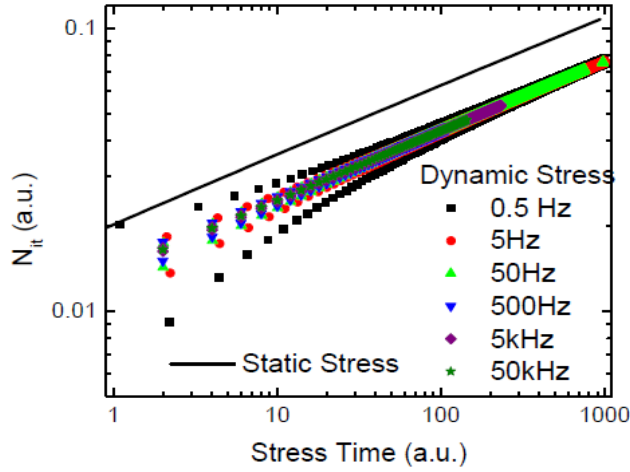


Fig. 2.4.2. Dynamic NBTI degradation simulated using RD model. The maximum and minimum ΔV_{th} became frequency independent in the long term region.

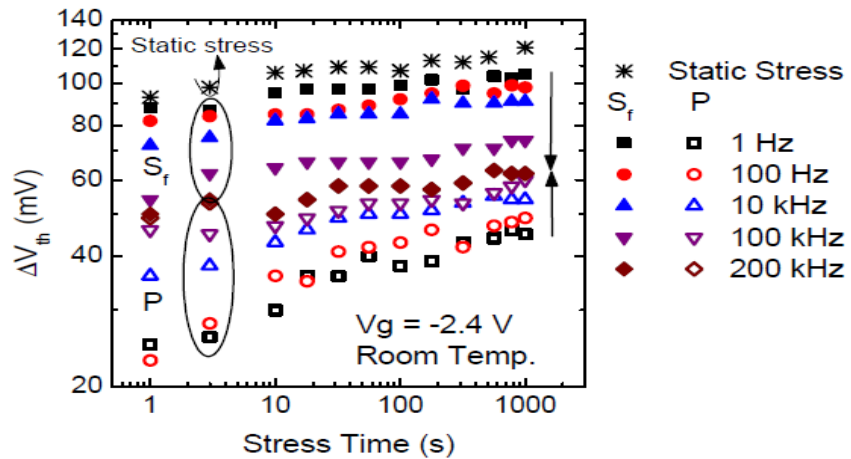


Fig. 2.4.3. Experimental results of dynamic ΔV_{th} under AC stress with various frequencies. The difference between the max and min ΔV_{th} is distinguished and never merged even after several stress/recovery cycles.

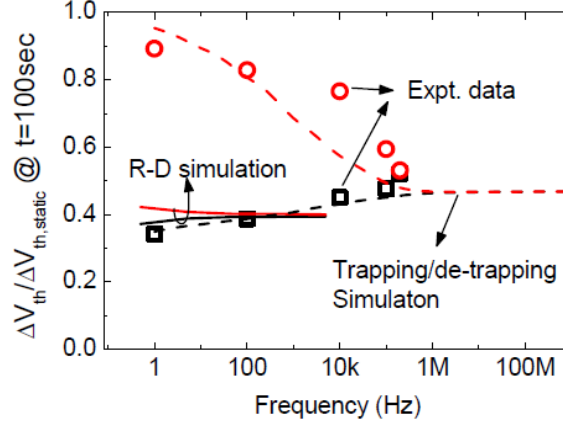


Fig. 2.4.4. The frequency dependence of ΔV_{th_max} and ΔV_{th_min} predicted by hole-trapping model, which shows much higher accuracy than the RD model.

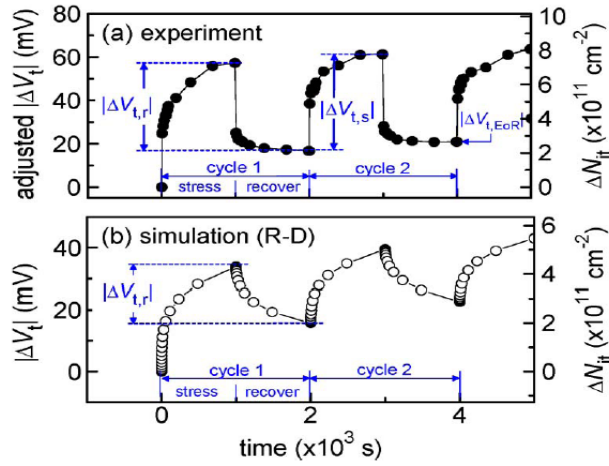


Fig. 2.4.5. (a) Dynamic NBTI degradation caused by interface-state generation. (b) Simulated result of ΔV_{th} using the reaction-diffusion.

The accuracy of the RD model is further challenged by measuring the dynamic NBTI degradation during multi stress/recovery cycles [2.17, 2.18]. The result shows that the recoverable ΔV_{th} keeps constant during each period, and independent of the number of the stress/recovery cycles. Such result is inconsistent with the RD model.

Fig. 2.4.5 shows the measurement and simulation result obtained from RD model. If the reaction-diffusion is the main domination of V_{th} degradation, both stress and recovery characteristics of the ΔV_{th} should follow the power-law relationship with recovery time with exponent of 1/6. Observed from Fig. 2.4.5(b), although the RD model is approximately consistent with the measured data during the stress process, a much slow recovery is predicted, which evidently deviates from the fast recovery in the initial stage observed from

measurement (Fig. 2.4.5(a)).

The recoverable ΔV_{th} component of both measurement and RD model result are extracted as a function of stress/recovery (SR) cycle number x , as shown in Fig. 2.4.6(a). Corresponding to the hydrogen diffusion model, the recoverable ΔV_{th} shows a monotonous decrease with increased SR cycle number. This behavior is because that during each recovery period, it is impossible for the diffused hydrogen molecules recover completely. Hydrogen molecules continuously diffuse into the gate oxide and even move out of the gate dielectrics. Therefore, the hydrogen density at the Si/SiO₂ interface decreases after several SR cycles, and results in the reduction of hydrogen density for stress and recovery transportation. However, such hypothesis is evidently inconsistent with the measurement result with constant recovery component, indicating that the hydrogen diffusion theory itself is not suitable for explaining the dynamic NBTI degradation.

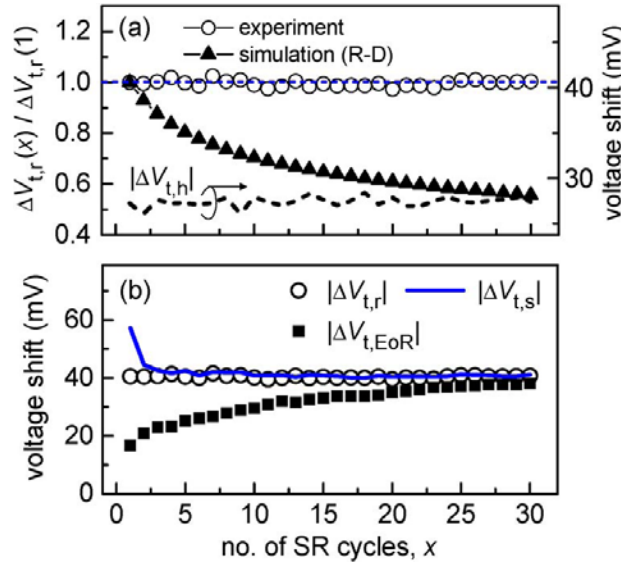


Fig. 2.4.6. (a) Measurement and RD model result of the recoverable ΔV_{th} during several SR cycles. The constant recoverable component is unable to support the hypothesis of RD model that the recoverable ΔV_{th} decreases monotonously with increase SR cycle. (b) The stress degradation component ($\Delta V_{t,s}$), recovery component ($\Delta V_{t,r}$) and the minimum point at the end of recovery ($\Delta V_{t,EoR}$).

In order to further study the nature of the dynamic NBTI degradation, the stress degradation ($\Delta V_{t,s}$) and the ΔV_{th} at the end of the recovery ($\Delta V_{t,EoR}$) during each SR cycle are extracted in Fig. 2.4.6(b). Except several cycles in the initial stage, the $\Delta V_{t,s}$ almost equals to the recoverable component ($\Delta V_{t,r}$). Such phenomenon indicates a charging-discharging

characteristic of the hole-traps at the interface. E' center ($O_3 \equiv Si^+ \cdot Si \equiv O_3$) has been widely accepted as defect for hole-trapping and detrapping [2.19]. For nitrated SiO_2 , the role of the k_N center ($N_3 \equiv Si^+ \cdot Si \equiv N_3$) as a switching hole trap has been suggested [2.20]. The continuously increased $\Delta V_{t,EoR}$ indicates that holes are trapped in the deep energy level and difficult to release.

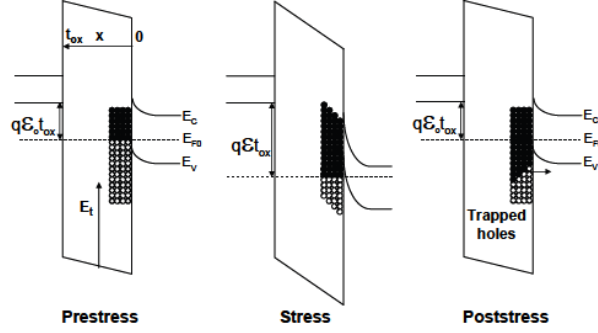


Fig. 2.4.7. Energy band diagrams of hole-trapping/detrapping characteristics. Prestress: trap sites are empty. Stress: holes are injected from the substrate into the gate oxide, and fill the empty trap sites. Poststress: holes trapped at the shallow energy levels are released and re-enter into the substrate. Those trapped at the deep level are difficult to escape, resulting in permanent degradation.

The typical band diagram for hole-trapping-detrapping characteristic is illustrated in Fig. 2.4.7 [2.21]. Initially, the trap sites are empty when no stress is applied to the gate. Under negative stress bias, holes are injected into the gate oxide and captured by the traps. After the stress is removed, Holes trapped in the shallow energy level are released and re-enter the substrate. Some of them are trapped in the deep level are difficult to escape, acting as permanent (unrecoverable) degradation.

The total ΔV_{th} is calculated using the hole-trapping model by integrating the traps distributed over all energy level and gate oxide thickness. A logarithmic stress time dependence of ΔV_{th} is derived [2.21, 2.22].

$$\Delta V_{th}(t) = \phi [A + B \log(1 + Ct)] \quad (2.4.1)$$

The analysis of measured data demonstrates that the hole-trapping model usually dominates the short term region of the NBTI degradation, and the power-law hydrogen diffusion model dominates the long term degradation. The combination of both mechanisms shows a good agreement with the measurement data using fast measurement technology, as

illustrated in Fig. 2.4.8 [2.23]. The data measured with large delay time features a power-law time function, consistent with previously developed RD model.

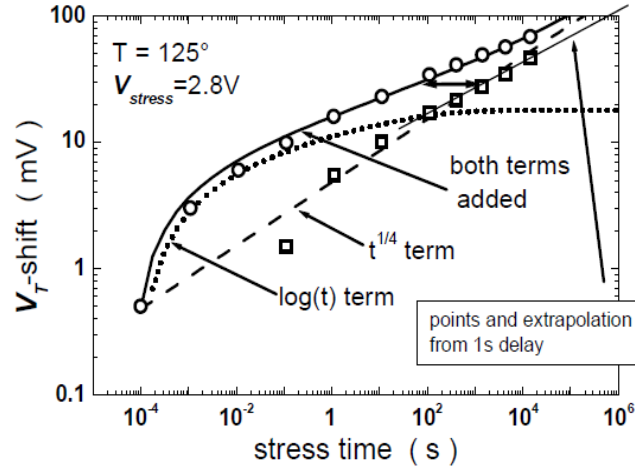


Fig. 2.4.8. Measurement results using fast (circle symbol) and slow (square symbol) technologies. By compared with the NBTI model, the logarithmic hole-trapping model dominates the short term region, while the power-law hydrogen diffusion model dominates the long term degradation.

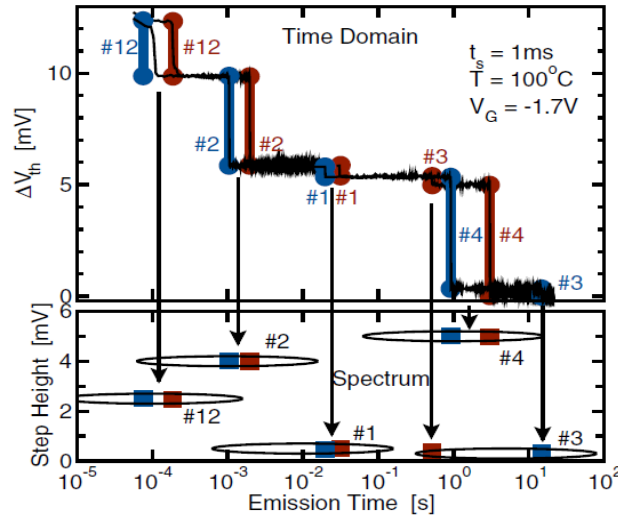


Fig. 2.4.9. Typical V_{th} recovery of a previously stressed small p-MOSFET. The black lines with slight noise in the top figure is the measurement result. The blue and red thick lines together with symbols in the bottom figure illustrate the extracted emission times and step heights corresponding to individual defect.

Recently, energy transfer theory proposed by T. Grasser et al. has become one of significant branch for explaining the NBTI effect. The defect behavior and capture/emission time of individual defect are capable to be monitored by using the time dependent defect spectroscopy (TDDS) technology. For the technology, the device is repeatedly stressed and

recovered for numbers of cycles. The statistic properties of the discrete steps during the recovery process are analyzed by studying the step heights (d) and emission time (τ_e), as illustrated in Fig. 2.4.9 [2.24]. The step heights are demonstrated independent of the microscopic defect state, but rather dependent on the interaction between the lateral positions of the defects.

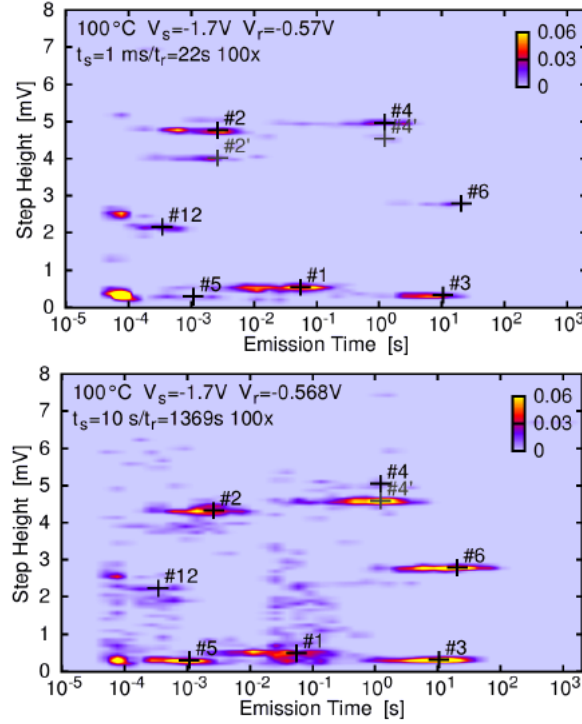


Fig. 2.4.10. TDDS spectral maps at two stress times, $t_s=1\text{ms}$ (top) and $t_s=10\text{s}$ (bottom). With increased stress time, the number of defect increases, and the defects with capture time $\tau_{c_ave} < t_s$ have great possibilities to be charged during the stress process.

The examples for TDDS spectral maps are obtained from two p-MOSFETs with 2.2nm nitride gate oxide. The measurement conditions are with -1.7V stress bias and 100°C temperature [2.24]. The results are shown in Fig. 2.4.10 [2.25]. The intensity of the (τ_e , d) clusters typically follows the function of stress bias and time duration ($P_c=1-\exp(-t_s/\tau_{c_ave}(V_{\text{stress}}))$), here $\tau_{c_ave}(V_{\text{stress}})$ indicates the average capture time at the stress bias of V_{stress} . With increased stress time, the number of defect increases, and the defects with capture time $\tau_{c_ave} < t_s$ have great possibilities to be charged during the stress process.

The increase of defect is considered due to the capture and emission mechanisms of the gate oxide traps. The microscopic model is illustrated in Fig. 2.4.11 [2.26, 2.27]. In the

initial state, the Si-O bonds are combined as neutral chemical bonds (state 1). When stress is applied, the Si-Si bonds are possibly to be transferred into neutral metastable state (state 2') and then dissociated to a positively charged stable state. When the surface is transferred to accumulation or during the measurement, the defects may exchange charges with substrate, and reform the metastable state (state 1'), which is invisible from the ΔV_{th} measurement.

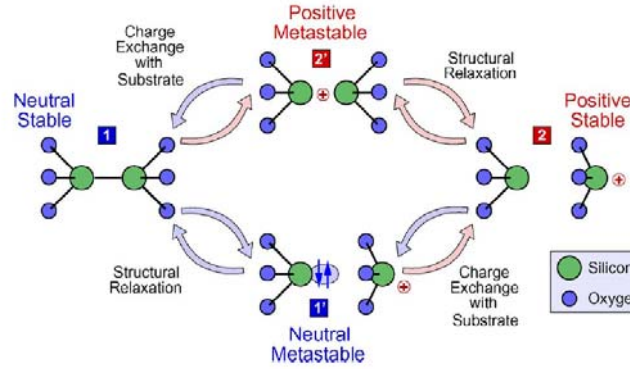


Fig. 2.4.11. Transfer of four states of the defects during the stress and recovery processes.

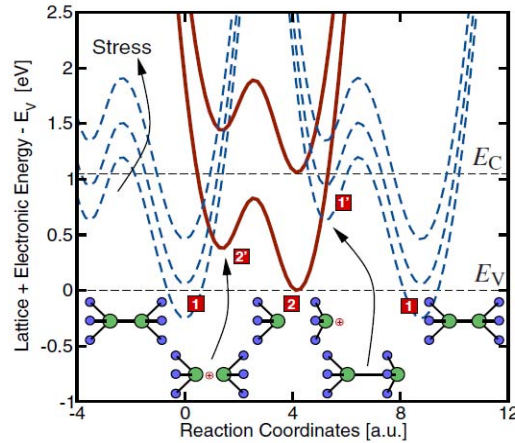


Fig. 2.4.12. Energy potential diagram corresponding to the four defect states.

The band diagram of the four-state charge exchange mechanism is shown in Fig. 2.4.12. The E center is assumed as the main component of the defect. Among the four states, two of them are electrically neutral (state 1 and 1') and two of them are positively charged (state 2 and 2'). Each state occupies one energy-well. Comparing to the stable state, the metastable state locate at higher energy level. Charge exchange mainly occurs between 1 and 2' as well as 2 and 1'. Moreover, the exchange between 1 and 1' as well as 2 and 2' are assumed to be purely thermally activated. The introduction of state 1' is for the purpose of explaining the

bias dependence of the hole-capture time constant observed in the microscope measurement [2.24, 2.28].

2.5 Summary

This section summarized the main NBTI model published during the past 10 years. The hydrogen reaction-diffusion (RD) model is simple to understand but based on numerous hypothesizes. Especially for nanoscale MOSFETs, the limitation of fabrication structure needed to be considered in the predictive model. Recently, with the improvement of the ultra fast measurement technologies, RD model began to show its drawback on describing the short term region degradation and recovery of measurement results. The hydrogen diffusion theory is challenged by hole-trapping theory. A logarithmic time dependent ΔV_{th} degradation is obtained by integrating the trap distributed in the gate oxide. The trap generation is demonstrated using TDDS measurement and explained from the view of energy transfer theory.

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Chapter 3 Reaction-Limited-Diffusion (RLD) NBTI Model

3.1 Introduction

The negative bias temperature instability (NBTI) effect is known as a significant concern of p-MOSFET reliability issues due to its serious impact on threshold voltage (V_{th}), drain-source current (I_{ds}), transconductance (g_m), subthreshold swing (SS) and even on the circuit performance [3.1-8]. The causation of the p-MOSFET degradation is widely accepted as the generation of positively charged interface states at the Si/SiO₂ interface and the increase of the gate oxide traps. Two theories explaining the NBTI degradation have been proposed. One is the reaction- diffusion (R-D) theory, which explains that the threshold voltage degradation (ΔV_{th}) is mainly caused by the breaking of Si-H bonds at the Si/SiO₂ interface and the following diffusion of H-H₂ species into the gate dielectrics. The R-D model describes ΔV_{th} with a power-law function of stress time as $\Delta V_{th} \sim A(T, E_{ox})t^n$ [3.1]. Here, $A(T, E_{ox})$ is strongly dependent on the temperature and the electric field in the oxide. Although the diffusion of H and H₂ is assumed to take place in the short-term and long-term stress regions, respectively, but an analytical solution is not provided [3.9]. The other well known theory is based on the trapping of holes. It considers that holes tunnel from the Si-substrate into the gate oxide and that these holes are then captured by pre-existing traps located inside the gate oxide [3.10]. A logarithmic function of time ($\Delta V_{th} \sim \log(t)$) has been developed, which is able to well explain the short term stress and the recovery processes [3.11]. However, besides of insufficient physical explanation, the applied empirical $\log(t)$ related model is unable to describe the V_{th} degradation due to H₂ diffusion during long-term stress processes [3.12]. Fig. 3.1 illustrates the drawback of both RD model and hole-trapping model by comparing with the measured data [3.9] using advanced fast measurement technology. The R-D model shows difficulties in describing the short term degradation and the hole trapping model shows obvious deviations in the long term stress region. In order to obtain a better overall fitting capability, another empirical model was developed by simply summing up different

degradation models ($\Delta V_{th}(t) = A \log(t) + Bt^n$) [3.13]. Unfortunately, the physical meaning for various NBTI models is not thoroughly investigated yet.

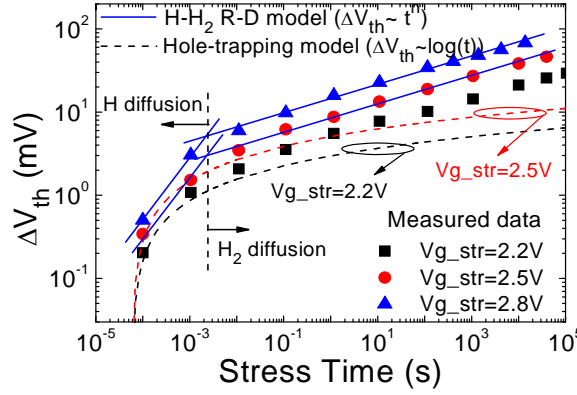


Fig. 3.1.1. Measured ΔV_{th} using an ultra-fast technique [3.9] in comparison to different NBTI models. The classical R-D model shows discontinuous time exponents between short-term and long-term stress regions. On the other hand, the hole-trapping model [3.12] has difficulties in describing the long-term stress region.

In this chapter, the NBTI degradation mechanisms are investigated in detail, and a unified reaction-limited- diffusion (RLD) model is newly developed for circuit aging simulation valid even after ultra long term circuit usage. Both reaction-diffusion and hole-trapping mechanisms are considered to reproduce the NBTI degradation over a wide range of stress duration and bias conditions. Then this NBTI model is implemented into the advanced compact MOSFET model HiSIM [3.14, 3.15], enabling a consistent simulation under dynamic operation of the real circuits.

3.2 Model Development

3.2.1 Reaction-Limited-Diffusion (RLD) Model

The principle of the developed reaction-limited-diffusion (RLD) model is illustrated in Figs. 3.2.1 and 3.2.2 [3.16]. By applying a negative gate stress bias to the p-MOSFET, a chemical reaction occurs between Si-H bonds and injected holes in the short initial period of stress process (Fig. 3.2.1 (a)). H atoms are released from the broken Si-H bonds and diffuse into the poly-silicon (poly-Si) gate where they form molecular H_2 [3.17]. Large numbers of Si

dangling bonds are generated, which dominate in the short term ΔV_{th} . Since the diffusion constant in SiO_2 is much larger than that in poly-Si [3.16], most of the H atoms stay in the SiO_2 and only some of them diffuse into the poly-Si during long-term stress (Fig. 3.2.1(b)). Therefore, the most significant ΔV_{th} shift occurs at the beginning of the short-term stress region due to the reaction process, and ΔV_{th} increases only slowly during the long term H_2 diffusion.

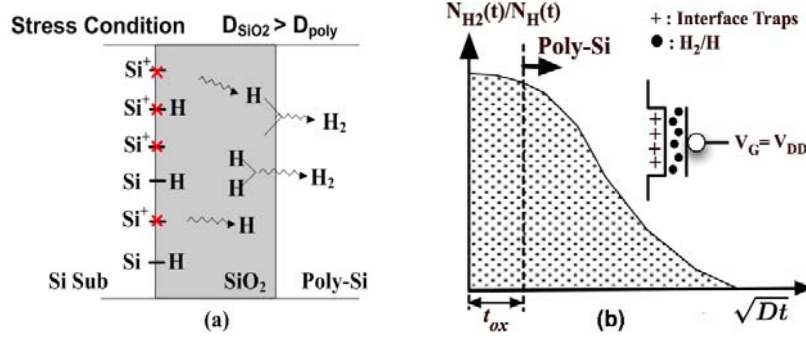


Fig. 3.2.1. Illustration of stress process. (a) Reaction of Si-H bonds occurs during the short term stress. H atoms diffuse away and penetrate into the poly gate. The diffusion constant in the SiO_2 (D_{SiO_2}) is larger than in the poly-gate (D_{poly}) (b) High density of H atoms in the SiO_2 acts as a source for long term H_2 diffusion in the poly-gate.

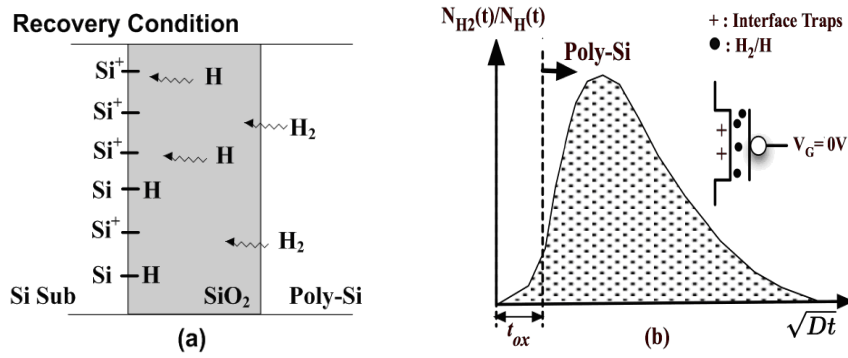


Fig. 3.2.2. Illustration of recovery process. (a) H atoms located in the SiO_2 repair the dangling Si-bonds within a short time, but those in the poly gate take a long time to diffuse back. (b) H atom density in SiO_2 decreases very fast while the H_2 density in the poly gate still keeps a similar value at the end of the stress.

After the stress is removed, the H atoms which remain in the SiO_2 are able to repair the Si dangling bonds within a very short time (Fig. 3.2.2(a)) and cause a fast recovery of ΔV_{th} . However, the H_2 molecules located in the poly silicon take a long time to diffuse back into SiO_2 or even flow out to the electrode, which results in a slow diffusion-limited recovery (Fig. 3.2.2(b)).

Neglecting the reverse reaction, generation of the interface state is described by the reaction equation (Eq. (3.2.1)) [3.18].

$$\frac{dn_T}{dt} = k_f (N_T - n_T) \quad (3.2.1)$$

Here n_T is the interface state density generated by the NBTI effect. k_f is the forward reaction rate and N_T is the total number of Si-H bonds. Assuming that n_T is much smaller than N_T in the initial stage, Eq. (3.2.1) is simplified as $dn_T/dt = k_f N_T$. Since the diffusivity of H_2 in the poly-Si is much lower than that in the SiO_2 [3.19], high concentration of H species is assumed to build up within the gate oxide and near the Si/ SiO_2 interface. As mentioned by ref. [3.18], a stable interface state is able to form only if H species diffuse away from the interface into gate oxide. Therefore, an increasing H_2 concentration in the SiO_2 suppresses the reaction process of Si-H bonds [3.6]. In this work, the forward reaction rate is assumed as an inverse function of the stress time ($k_f \sim 1/t$), which is able to consistently describe the reverse diffusion in the classical RD model [3.1]. Since k_f is reported as an exponential function of the gate oxide electric field E_{ox} [3.1], it is reasonable to write k_f as $k_f = R_{Eox}^S / t$, where R_{Eox}^S is the reaction coefficient determined by E_{ox} . By substituting the expression for k_f into Eq. (3.2.1) and solving the equation, the ΔV_{th} induced by reaction mechanism ($\Delta V_{th_rea}^S$) is derived as

$$\Delta V_{th_rea}^S(t) = \frac{q}{C_{ox}} \cdot n_T(t) = \frac{q N_T}{C_{ox}} \cdot R_{Eox}^S \log\left(\frac{t}{\tau_{str}}\right) \quad (3.2.2)$$

Here q is the electron charge, C_{ox} is the equivalent oxide capacitance and τ_{str} is the reaction time constant which indicates the lower limit of the reaction time. If $t < \tau_{str}$, the Si-H bond reaction mechanism becomes invalidated. The H_2 molecules generated from the Si-H bond reaction act as the source of the diffusion process. The diffusion model in the gate oxide is written as

$$\Delta V_{th_diff}^S(t) = \Delta V_{th_rea}^S(t) \cdot \left(D_{SiO_2} t\right)^{1/6} \quad (3.2.3)$$

Since the diffusion species is assumed to be H_2 , the power exponential of the stress time is selected as 1/6 [3.7]. D_{SiO_2} is the H_2 diffusion constant in the oxide. After arriving at the SiO_2 /poly-Si interface, H_2 molecules further diffuse into the poly-Si. Based on the diffusion theory [3.20], the H_2 density distribution within the SiO_2 and poly-Si (n_{H_2}) is calculated as

$$n_{H_2}(x, t) = n_{H_2_Si/SiO_2} \operatorname{erfc} \left(\frac{x}{2\sqrt{D_{SiO_2}t}} \right) \quad (3.2.4)$$

Here x is the distance away from the Si/SiO₂ interface, and $n_{H_2_Si/SiO_2}$ is the H₂ density at Si/SiO₂ interface. The diffusion time dependence of the H₂ distribution in the gate oxide and poly-Si gate is shown in Fig. 3.2.3. In the following, we define t_{1s} as the time that H₂ diffuses from Si/SiO₂ to SiO₂/poly-Si interface. According to the diffusion theory, t_{1s} is calculated as [3.6]

$$T_{ox} = \sqrt{2D_{SiO_2}t_{1s}} \Rightarrow t_{1s} = \frac{T_{ox}^2}{2D_{SiO_2}} \quad (3.2.5)$$

If $t < t_{1s}$, the diffusion of H₂ mainly occurs in the gate oxide and the RLD model is written as in Eq. (3.2.3). If the stress time increases to $t > t_{1s}$, the H₂ density at the SiO₂/poly-Si interface increases rapidly to that at the Si/SiO₂ interface within 0.1s, and the H₂ diffusion in the poly-Si gate is taken into account, as shown in Eq. (3.2.6).

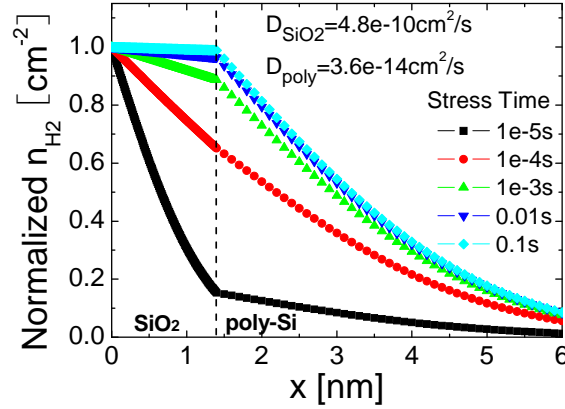


Fig. 3.2.3. The stress time dependence of the H₂ density into the gate direction (x).

The stress ΔV_{th} induced by RLD ($\Delta V_{th_RLD}^S$) is finally written as

$$\begin{aligned} \Delta V_{th_RLD}^S(t) &= \Delta V_{th_rea}^S(t) + \Delta V_{th_diff}^S(t) \\ &= \begin{cases} \left[\frac{qN_T}{C_{ox}} \cdot R_{Eox}^S \cdot \log\left(\frac{t}{\tau_{str}}\right) \left[1 + (D_{SiO_2}t)^{1/6} \right] \right] & (0 < t < t_{1s}) \\ \left[\frac{qN_T}{C_{ox}} \cdot R_{Eox}^S \cdot \log\left(\frac{t}{\tau_{str}}\right) \left[1 + (D_{SiO_2}t_{1s})^{1/6} + \operatorname{erfc}\left(\frac{T_{ox}}{2\sqrt{D_{SiO_2}t}}\right) (D_{poly}t - t_{1s})^{1/6} \right] \right] & (t > t_{1s}) \end{cases} \quad (3.2.6) \end{aligned}$$

Considering that the gate oxide thickness in most of the nanoscale MOSFETs is very small, moreover, the Si-H bond reaction dominates the V_{th} degradation in the initial stage, it is reasonable to neglect the H_2 diffusion in the gate oxide. Therefore, the RLD model can be simplified as

$$\Delta V_{th_RLD}^S(t) = \frac{qN_T}{C_{ox}} \cdot R_{Eox}^S \cdot \log\left(\frac{t}{\tau_{str}}\right) \left[1 + (D_{poly}t)^{1/6}\right] \quad (3.2.7)$$

After the stress is removed, H_2 remaining in the SiO_2 diffuses back to repair the Si dangling bonds, which leads to a fast recovery (ΔV_{ox}^R). Since the association of Si dangling bonds is much faster than the H_2 diffusion, the recovery is controlled by diffusion process in the initial stage. Here we define t_{1r} as the H_2 back diffusion time from SiO_2 /poly-Si to Si/ SiO_2 interface. For recovery times $t < t_{1r}$, the back diffusion of H_2 in the oxide dominates the recovery. When $t > t_{1r}$, H_2 molecules located in the poly-Si gate begin to diffuse back. However, some of these H_2 molecules continue to diffuse forward to the gate electrode, which reduces the H_2 back-diffusion density and reduces the recovery rate. The recovery ΔV_{th} ($\Delta V_{th_RLD}^R$) in the initial ($0 < t < t_{1r}$) and long term ($t > t_{1r}$) regions are written as

$$\Delta V_{th_RLD}^R(t) = \begin{cases} \Delta V_{th_max}^S - \Delta V_{th_ox}^R(t) & (0 < t < t_{1r}) \\ = \Delta V_{th_max}^S - \Delta V_{th_ox}^S \cdot \left[\xi D_{SiO_2} t\right]^{1/6} \cdot R_{rec} \log\left(\frac{t}{\tau_{rec}}\right) & \\ \Delta V_{th_max}^S - \Delta V_{th_ox}^R(t_{1r}) - \Delta V_{th_poly}^R(t) & (t > t_{1r}) \\ = \Delta V_{th_max}^S - \Delta V_{th_ox}^S \cdot \left(\xi D_{SiO_2} t_{1r}\right)^{1/6} \cdot R_{rec} \log\left(\frac{t_{1r}}{\tau_{rec}}\right) & \\ - \Delta V_{th_poly}^S (1 - D_{poly}t)^{1/6} \cdot R_{rec} \log\left(\frac{t - t_{1r}}{\tau_{rec}}\right) & \end{cases} \quad (3.2.8)$$

Here $\Delta V_{th_ox}^R$ and $\Delta V_{th_poly}^R$ are defined as the ΔV_{th} recovery induced by the H_2 back diffusion from SiO_2 and poly-Si. $\Delta V_{th_max}^S$, $\Delta V_{th_ox}^S$ and $\Delta V_{th_poly}^S$ are respectively defined as the maximum ΔV_{th} at the end of stress without recovery, ΔV_{th} induced by H_2 diffusion in the gate oxide and poly-Si during stress process. ξ is the reverse diffusion coefficient for data fitting [3.6, 3.21]. R_{rec} is the recovery rate coefficient. τ_{rec} is the Si dangling bond annealing time constant. The relationship between $\Delta V_{th_max}^S$, $\Delta V_{th_ox}^S$ and $\Delta V_{th_poly}^S$ is shown in Eq. (3.2.9) with stress time $t = t_s$.

ΔV_{th} . The ΔV_{th} degradation is induced by two components: holes trapped at the interface traps and holes tunneling into the gate oxide [3.22]. Moreover, the charge exchange between interface states and channel is a faster process than tunneling [3.23], indicating that hole-trapping and de-trapping is the main mechanism in the initial stress and recovery stage. The hole trapping rate in the interface states (dn_{T_int}/dt) is written as

$$\frac{dn_{T_int}(t)}{dt} = k [N_{IT} - n_{T_int}(t)] \quad (3.2.10)$$

where N_{IT} is the total density of interface traps, n_{T_int} is the density of trapped holes and k is the capture rate of the interface traps. The interface state density is derived by solving Eq. (3.2.10) as

$$n_{T_int}(t) = N_{IT} [1 - \exp(-kt)] = N_{IT} \left[1 - \exp\left(-\frac{t}{\tau_c}\right) \right] \quad (3.2.11)$$

Here $\tau_c = 1/k$ is the capture time, which is proportional to the electric field in the gate oxide [3.24].

For the bulk oxide hole trapping, the generation of K-center defects (silicon dangling bond defect back bonded with three nitrogen atoms) located within the gate dielectric is considered mainly responsible for ΔV_{th} . The precursor of the K-center with small dissociation energy [3.25] splits into a neutral silicon dangling bond and a positively charged silicon atom [3.26] after capturing a hole which tunnels from the substrate. The charge transmission coefficient (T_{tunnel}) is written as [3.26]

$$T_{tunnel} = \exp\left(-2\sqrt{\frac{2m^*}{\hbar^2}} E_t x_m\right) = \exp(-2\beta x_m) \quad (3.2.12)$$

$$\beta = \sqrt{\frac{2m^*}{\hbar^2}} E_t \quad (3.2.13)$$

where m^* is the effective electron mass, x_m is the distance between the trap position and the SiO₂/Si interface, E_t is the barrier height, \hbar is the Planck constant divided by 2π and β is a constant. With increased stress time, the increased concentration of positively charged K-centers reduces the potential difference in the gate dielectric. As verified by experiments, the response of K-centers is proportional to the gate potential [3.25]. Following the calculation methodology described in [3.25], T_{tunnel} can be approximated as an inverse

function of stress time [3.26, 3.27].

$$T_{tunnel} = \exp(-2\beta x_m) = \frac{\tau_0}{t} \quad (3.2.14)$$

In Eq. (3.2.14), $\tau_0 = 3 \cdot 10^{-4}$ s is the trap generation time constant. The trap distribution in the gate oxide is written as $N(x) = N_0 e^{\lambda x}$ [3.27], where N_0 is the concentration of tunneling holes and λ is the attenuation coefficient in the oxide. Thus the total generated trap density (n_{T_ox}) is derived as

$$n_{T_ox} = \int_0^{x_m(t)} N(x) dx = \int_0^{x_m(t)} N_0 e^{\lambda x} dx = \frac{N_0}{\lambda} \left\{ \exp \left[\ln \left(\frac{t}{\tau_0} \right)^{\frac{\lambda}{2\beta}} \right] - 1 \right\} = \frac{N_0}{\lambda} \left(\frac{t}{\tau_0} \right)^n \quad (3.2.15)$$

If $\lambda = 2 \text{ nm}^{-1}$ and $\beta = 7.24 \text{ nm}^{-1}$, the time exponent is calculated as $n = \lambda / (2\beta) = 0.14$ [3.26]. The final expression for the hole trapping induced ΔV_{th} is obtained by combining Eq. (3.2.11) and Eq. (3.2.15)

$$\Delta V_{th_HT}^S = \frac{q}{C_{ox}} (n_{T_int} + n_{T_ox}) \approx \frac{q}{C_{ox}} \left\{ N_{IT} \left[1 - \exp \left(-\frac{t}{\tau_c} \right) \right] + \frac{N_0}{\lambda} \left(\frac{t}{\tau_0} \right)^{0.14} \right\} \quad (3.2.16)$$

After the stress is removed, the recovery ΔV_{th} is written as

$$\Delta V_{th_HT}^R = \frac{q N_{it}}{C_{ox}} \left[1 - \exp \left(-\frac{t_s}{\tau_c} \right) \right] \exp \left(-\frac{t-t_s}{\tau_e} \right) + \frac{q N_0}{C_{ox}} \left(\frac{t_s}{\tau_0} \right)^{0.14} \left[1 - \left(\frac{t-t_s}{\tau_0} \right)^{0.14} \right] \quad (3.2.17)$$

Here τ_e is the emission time constant. Both the Si-H bond reaction and the hole trapping effects comprehensively contribute to NBTI degradation. Therefore the unified model is written as

$$\Delta V_{th} = \Delta V_{th_RLD} + \Delta V_{th_HT} \quad (3.2.18)$$

The static and dynamic simulation result of the unified model is shown in the upper figure of Fig. 3.2.5 (a). The model parameters are selected arbitrarily within meaningful ranges. The stress condition dependence of model parameters is analyzed in the next section. The maximum ΔV_{th} (ΔV_{th_max}) and the recoverable ΔV_{th_rec} ($\Delta V_{th_rec} = \Delta V_{th_max} - \Delta V_{th_min}$) decrease with the increased stress frequency due to the reduction of the stress/recovery time during each cycle. The cycle number dependences of ΔV_{th_max} and ΔV_{th_rec} are shown in the lower part of Fig. 3.2.5(a), which is consistent with the recent experimental observation [3.28]. Fig. 3.2.5(b) shows the contributions of the RLD, hole trapping and the unified model to the

AC NBTI degradation. The simulation verifies that ΔV_{th} becomes frequency independent under higher frequency operation. This result is consistent with the reports in the previous works [3.29].

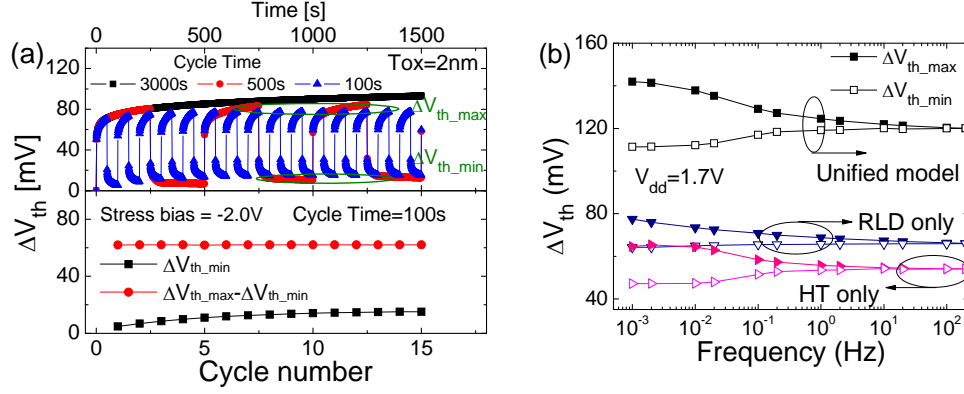


Fig. 3.2.5. (a) Upper: Static and dynamic NBTI effect simulated using the unified model. Lower: cycle number dependence of the ΔV_{th_min} and recoverable ΔV_{th} ($\Delta V_{th_max} - \Delta V_{th_min}$). (b) Frequency dependence of the RLD, HT and the unified NBTI model.

3.3 Model Verification

3.3.1 Model Verification for Various Bias Conditions

The unified NBTI model is verified using the experimental data from different literatures. The model parameters including constants and variables are listed in Table 3.3.1 and Table 3.3.2. The values are extracted by fitting the developed model with the experimental data [3.30].

Table. 3.3.1. Model parameters of the unified NBTI model

Stress model	Meaning	Value
τ_c [s]	Hole capture time constant	Table 3.3.2
R_{Eox}^S	Reaction rate under stress condition	Table 3.3.2
τ_{str} [s]	Reaction time constant	Table 3.3.2
N_0 [cm ⁻³]	Density of tunneling holes	Table 3.3.2
N_{IT} [cm ⁻²]	Interface state density	1.39e11
τ_0 [s]	Trap generation time constant	3e-4
N_T [cm ⁻²]	Maximum interface trap density	1e11

D_{SiO_2} [cm^2/s]	H ₂ forward diffusion constant in SiO ₂	4.8e-10
D_{poly} [cm^2/s]	H ₂ forward diffusion constant in poly-Si	3.6e-14
t_{1s} [s] (ref. [3.28])	H forward diffusion time in the gate oxide	1e-5
Recovery model	Meaning	Value
τ_{rec} [s]	recovery time constant	2e-4
ξ	Diffusion coefficient in SiO ₂ for data fitting	1e2
R_{rec}	Recovery rate coefficient	0.07
τ_r [s]	Hole emission time constant	1.4e-3
t_{1r} [s] (ref. [3.13])	H reverse diffusion time in the gate oxide	1e-3

Table. 3.3.2. Stress bias dependence of model parameters

	R_{Eox}^S	τ_{str}	τ_c	N_0
2.3V	0.034	4.76e-6	1.4e-3	2.16e17
2.1V	0.0235	6.67e-6	1.4e-3	2.16e17
1.9V	0.016	1.43e-5	1.4e-3	2.16e17
1.7V	0.009	3.33e-5	1.4e-3	2.16e17
1.5V	0.0025	5e-5	1.4e-3	2.16e17
1.3V	0.0014	6.67e-5	2.5e-3	1.23e17
1.2V	0.0014	6.67e-5	5e-3	4.31e16

Firstly, the RLD model and the HT model are discussed separately to show the stress dependence of these two mechanisms. As shown in Fig. 3.3.1(a), the RLD model results show good agreement with measurement [3.30] over a wide range of stress time from 10^{-5} s to 10^5 s under relative high stress bias ($V_{\text{g_str}}$). The existing empirical model [3.13] shows deviation in the long term region even when modifying parameters, indicating that such inaccuracy is not due to data fitting, but some physics is missing in the empirical model. When the stress voltage ($V_{\text{g_str}}$) is reduced to $V_{\text{g_str}} < 1.5\text{V}$, the RLD model exhibits significant deviations from the measurements under short term stress conditions, as shown in Fig. 3.3.1(b). The reason is

that, the Si-H bond breaking is significantly weakened under low gate oxide fields, and that hole trapping in the gate oxide becomes mainly responsible for the V_{th} degradation. Fig. 3.3.1(c) shows results calculated with the developed unified model, where the long term stress simulation is extended to 10 years.

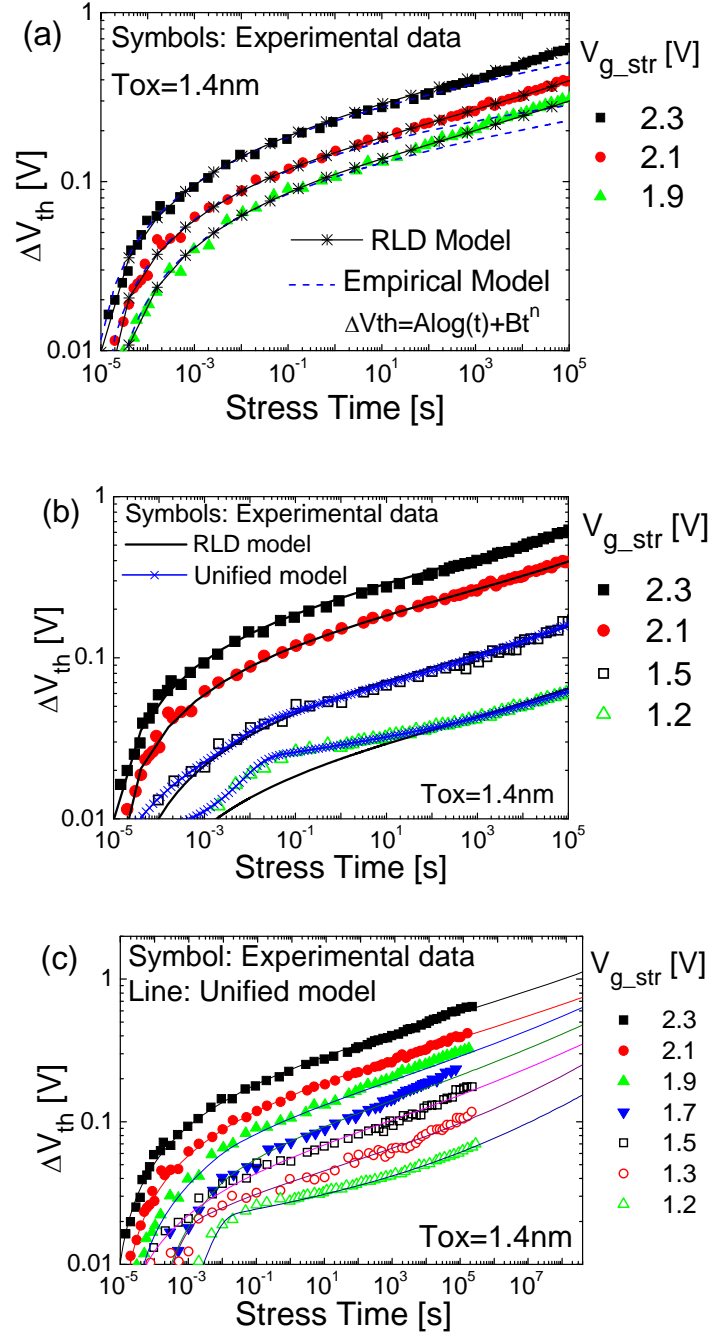


Fig. 3.3.1. (a) Comparison of RLD (solid line) and empirical model (dashed line) [3.13] with measured data [3.30]. (b) Calculation results from the RLD model and HT model under high and low stress bias. (c) Unified NBTI model results compared with measured data under stress voltage V_{g_str} ranging from 2.3V to 1.2V.

As observed from Table 3.3.2, with increased V_{g_str} , the reaction coefficient (R_{Eox}^S) increases and reaction time constant (τ_{str}) decreases. Such observation denotes that the Si-H bond reaction occurs more easily under high stress bias. When V_{g_str} is reduced to 1.3V, R_{Eox}^S and τ_{str} become V_{g_str} insensitive.

The developed unified NBTI model is demonstrated to be able to accurately predict also ΔV_{th} recovery data [3.13] over a wide time range, as shown in Fig. 3.3.2. The short term recovery is due to the rapid repairing of Si-dangling bonds by H atoms remaining in the gate oxide, and the long term recovery is due to the slow back-diffusion of H_2 molecules from the SiO_2 /poly-Si interface into the gate dielectrics. However, even in the recovery process, H_2 located at the SiO_2 /poly-Si interface continuously diffuse towards the gate electrode. Therefore, the recoverable H_2 density decreases and results in a less steep recovery in the long term region, as shown in Fig. 3.3.2(a). Fig. 3.3.2(b) shows a linear plot of ΔV_{th} recovery, where a significant fast recovery during the initial recovery time is clearly observed, and followed by a slow recovery for long recovery time. Model parameters of the recovery process are listed in Table 3.3.1.

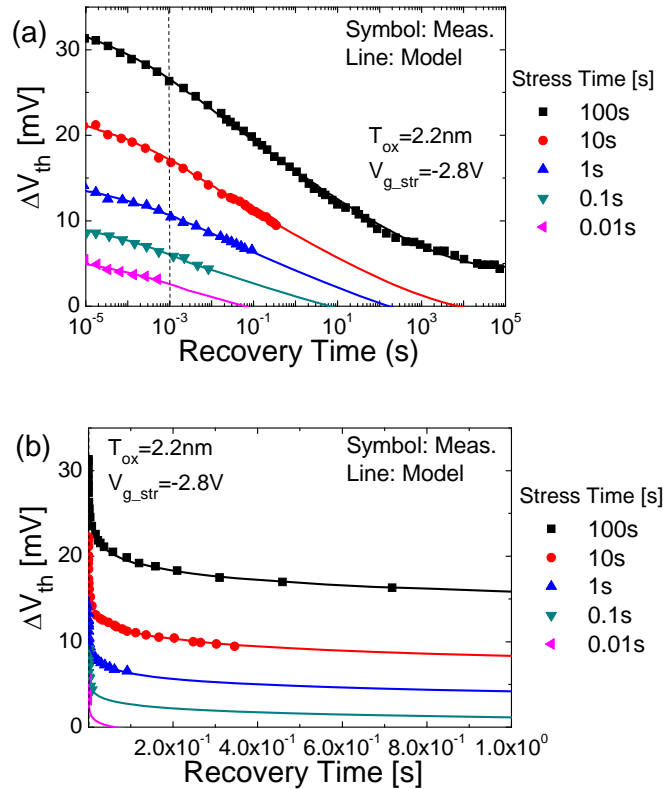


Fig. 3.3.2. (a) ΔV_{th} recovery characteristics plotted in semi-log scale. (b) ΔV_{th} recovery characteristics plotted in linear scale.

3.3.2 Model Verification for AC Stress

In order to simulate the circuit-performance degradation, the unified NBTI model is implemented into the advanced surface potential-based MOSFET model HiSIM to solve the time dependent degradation in a consistent way. Observed from the previous literatures, the NBTI effect mainly results in a parallel shift of the subthreshold current [3.31]. Therefore, the implementation of the NBTI degradation is done as a flat band voltage shift (ΔV_{fb}) in HiSIM. As shown in the flow chart in Fig. 3.3.3(a), the gate oxide field at the i^{th} time step t_i [$E_{ox}(t_i)$] is calculated from $V_{fb}(t_i)$ given by HiSIM model, here $E_{ox}(t_i) = (V_g - V_{fb}(t_i) - \phi_s(t_i)) / t_{ox}$, V_g is the gate voltage, ϕ_s is the surface potential at threshold condition and t_{ox} is the gate oxide thickness. Since R_{Eox} and R_{HT} in the RLD model and the HT model are E_{ox} dependent (see Table 3.3.2), ΔV_{fb} at t_i is calculated by $\Delta V_{th}(t_i)$, which is the function of $E_{ox}(t_i)$. Then $V_{fb}(t_{i+1})$ is calculated by adding $\Delta V_{th}(t_i)$ to $V_{fb}(t_i)$, and the gate electrical field changing from $E_{ox}(t_i)$ to $E_{ox}(t_{i+1})$.

The simulation method for ΔV_{th} under arbitrary E_{ox} is described in Fig. 3.3.3(b). The decision of stress or recovery is done by the sign (-/+) of E_{ox} . The time interval is Δt , thus $t_{i+1} = t_i + \Delta t$. Under a stress condition, the electrical field at the first time point $t_{s,1}$ is obtained as $E_{ox}(t_{s,1})$ by using HiSIM. The Si-H reaction rate $R_{Eox}(t_{s,1})$ and hole trapping rate $R_{HT}(t_{s,1})$ are obtained following the relationship shown in Table. 3.3.2, so that the threshold voltage shift at $t_{s,1}$ is calculated from Eq. 3.2.6 and Eq. 3.2.16 as $\Delta V_{ths}(t_{s,1}) = \Delta V_{th_RLD}[E_{ox}(t_{s,1})] + \Delta V_{th_HT}[E_{ox}(t_{s,1})]$. At the second time point $t_{s,2}$, the flat band voltage V_{fb} is shifted to $V_{fb}(t_{s,2})$ as $V_{fb}(t_{s,2}) = V_{fb}(t_{s,1}) + \Delta V_{ths}(t_{s,1})$. Therefore, calculated by HiSIM, E_{ox} is shifted to $E_{ox}(t_{s,2})$. The threshold voltage shift at $t_{s,2}$ is obtained as $\Delta V_{ths}(t_{s,2}) = \Delta V_{th_RLD}[E_{ox}(t_{s,2})] + \Delta V_{th_HT}[E_{ox}(t_{s,2})]$. Under stress bias, ΔV_{th} at i^{th} time point t_i is calculated by accumulating the previous results: $\Delta V_{th}(t_i) = \Delta V_{ths}(t_{s,1}) + \Delta V_{ths}(t_{s,2}) + \dots + \Delta V_{ths}(t_{s,i})$.

Under the recovery condition, since the recovery model parameters are insensitive to E_{ox} , ΔV_{th} recovery is calculated using Eq. 3.2.8 and Eq. 3.2.17 with the integrated recovery time ($t_{r,i} = t_{r,i-1} + \Delta t$), where $t_{r,i}$ and $t_{r,i-1}$ are the recovery time at i^{th} and $(i-1)^{\text{th}}$ step. ΔV_{th} during recovery is written as $\Delta V_{thr}(t_i) = \Delta V_{th_rec}(t_{r,i})$.

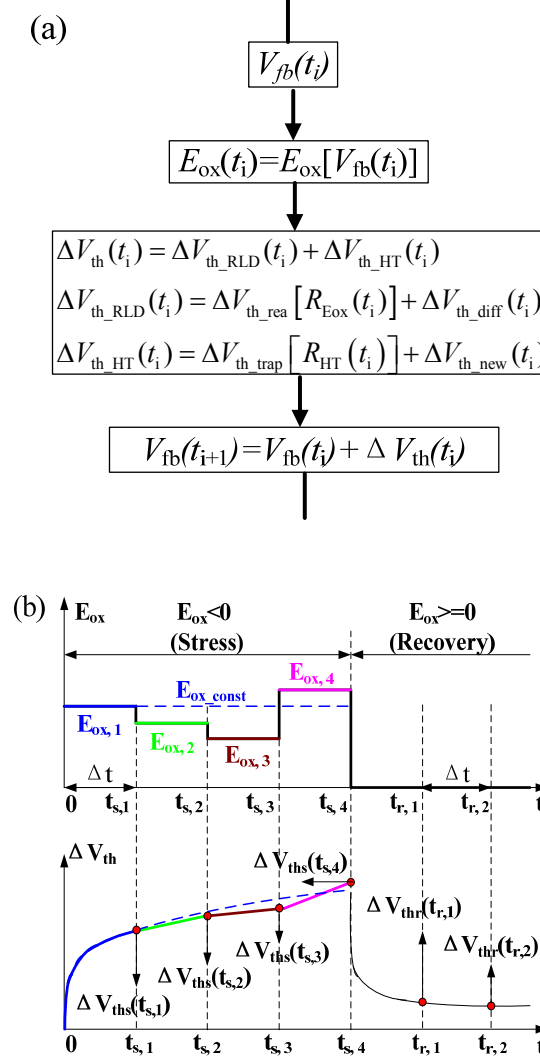


Fig. 3.3.3. (a) Flow chart of the flat band voltage ($V_{fb}(t_i)$) at i^{th} time point (t_i). **(b)** ΔV_{th} under various $E_{ox,i}$. Stress and recovery are distinguished by $(-/+E_{ox})$. At i^{th} stress time step ($t_{s,i}$), $\Delta V_{th}(t_i)$ is calculated as a function of $E_{ox,i}$ and $t_{s,i}$ by using the developed NBTI stress model ($\Delta V_{th}(t_i) = \Delta V_{th_str,i} = \Delta V_{th_str}(E_{ox,i}, t_{s,i})$), where $\Delta V_{th_str,i}$ is stress induced ΔV_{th}). When time changes to $t_{s,i+1} (=t_{s,i} + \Delta t)$ and E_{ox} changes to $E_{ox,i+1}$, ΔV_{th} is calculated based on the previous result ($\Delta V_{th_str,i}$) as $\Delta V_{th}(t_{i+1}) = \Delta V_{th_str,i} + \Delta V_{th_str,i+1}(E_{ox,i+1}, t_{s,i+1})$.

The developed R-D model is verified with dynamic NBTI data with 1000s stress and 1000s recovery duration [3.32] (Fig. 3.3.4 (a)). The device structure parameters are gate width $W=100\mu m$, gate length $L=120nm$ and oxide thickness $T_{ox}=2.8nm$. Stress voltage $V_{g_str}=-2.6V$, and temperature $TEMP=100^\circ C$ are chosen for the simulation. Good agreement of simulation and measurements is obtained during several stress and recovery cycles. Corresponding shift of gate current density (I_g) and drain current (I_{ds}) under dynamic NBTI stress are simulated in

Fig. 3.3.4 (b) and (c) by implementing the developed RLD model into the compact MOSFET model HiSIM. I_g and I_{ds} are solved in a consistent way, and their time-dependent degradation is due to the V_{th} degradation during each stress period. This behavior is explained by the shift of the flat band voltage (V_{fb}) (the simulation flow is shown in Fig. 3.3.3(a)). I_g and I_{ds} are therefore unable to remain constant during the simulation with the HiSIM model. When ΔV_{th} is simulated under a sine wave stress, a non-sine ΔV_{th} waveform is observed as shown in Fig. 3.3.4(d). Since the degradation of ΔV_{th} results from the integration effect over the complete stress time, the maximum value of ΔV_{th} is observed at the end of the stress period. This is the reason why the time-dependent waveform of ΔV_{th} in Fig. 3.3.4(a) and (d) differs from the time-dependent waveform of the stress input. For the sine waveform of the input stress, the change in ΔV_{th} flattens at the end of each positive stress period because the input stress gradually diminishes due to its sine waveform. Consequently, a non-sine waveform of the ΔV_{th} change results.

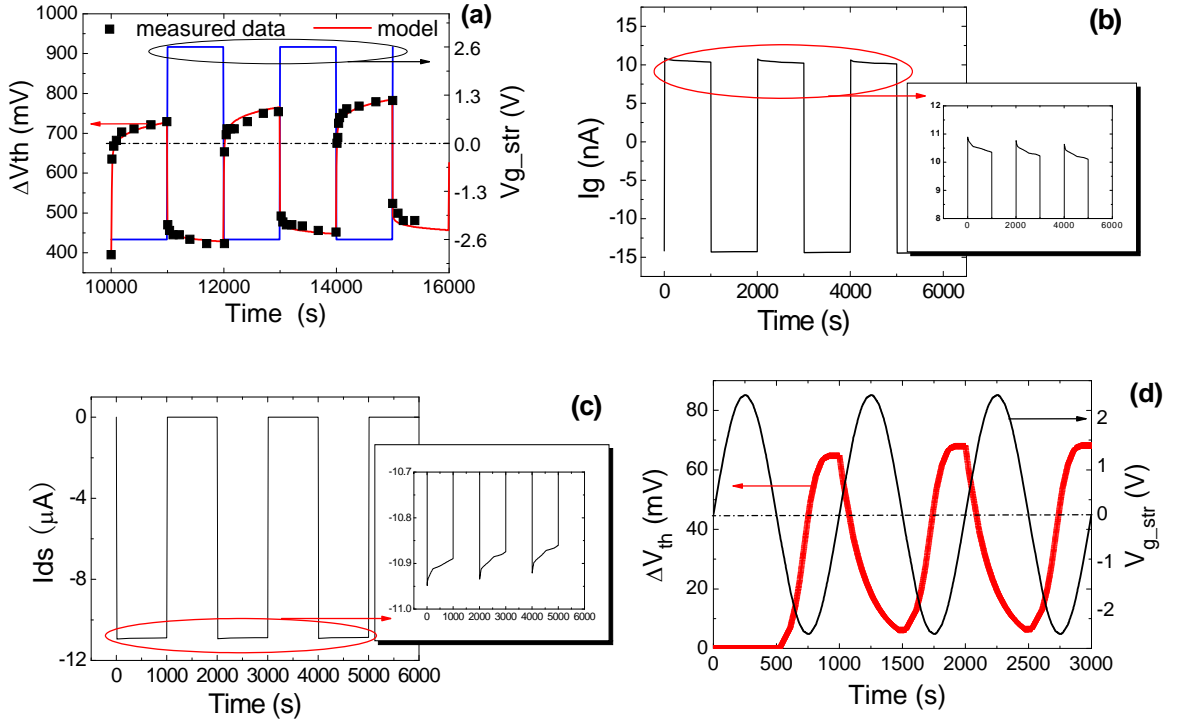


Fig. 3.3.4. (a) Shift of the threshold voltage under dynamic NBT stress with 1000s stress and 1000s recovery duration [3.32]. (b) NBTI induced gate current (I_g) degradation. (c) NBTI induced drain current (I_{ds}) degradation. (d) Simulation of sine wave stress and corresponding V_{th} degradation.

Under the AC stress, the ΔV_{th} is characterized by two specific values: the maximum

value (ΔV_{th_max}) and the minimum value (ΔV_{th_min}) observed during each stress-recovery cycle (defined in Fig. 3.2.5(a)). Experimental results of the AC NBTI degradation are shown in Fig. 3.3.5(a) as a function of cycle frequency, where the asymmetric frequency dependence of ΔV_{th_max} and ΔV_{th_min} has been observed as summarized in Fig. 3.3.5(b) [3.11]. With increased frequency, the number of dissociation Si-H bonds decreases during a stress/recovery cycle, which is observed as the decreased ΔV_{th_max} . An increased frequency also reduces the recovery time. Since the recovery in the initial stage is much slower than the Si-H bond reaction, the recoverable ΔV_{th} decreases and even disappears under high frequency condition. The dynamic NBTI effects on ΔV_{th_max} and ΔV_{th_min} are simulated with the developed unified NBTI model and compared with the measured data. Good agreement is observed over a wide range of frequencies.

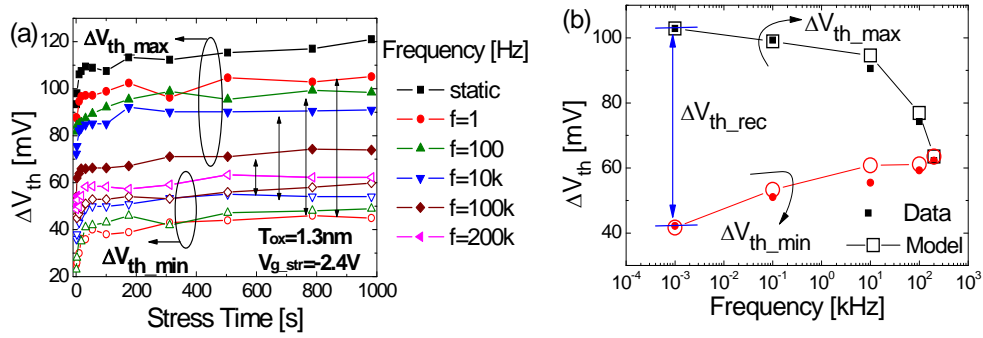


Fig. 3.3.5. (a) Experimental results of AC NBTI degradation for p-MOSFET samples with DPN SiON of 1.3nm EOT with stress bias $V_{g_str}=-2.4V$ [3.10]. (b) Frequency dependence of ΔV_{th_max} and ΔV_{th_min} .

The simulated duty cycle dependence of ΔV_{th} , depicted in Fig. 3.3.6, has a standard S-shape, which is consistent with the previous reports [3.33].

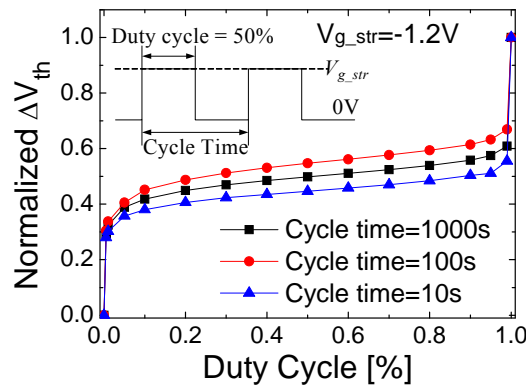


Fig. 3.3.6. Duty cycle dependence of ΔV_{th} .

3.4 Summary

A unified NBTI model including reaction-limited-diffusion (RLD) and hole trapping (HT) effects is developed and verified against experimental data to predict static and dynamic NBTI degradation, including the observed degradation recovery effects, over a wide range of stress time durations, bias conditions and dynamic stress frequencies. Thorough investigation of the measured degradation data indicates that, although both RLD and HT contribute to the ΔV_{th} degradation, RLD dominates the high stress degradation while HT is the main mechanism under low stress conditions. The developed NBTI model is implemented into the surface-potential based MOSFET model HiSIM for degradation prediction the current degradation in a consistent way by changing the flat band voltage.

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Chapter 4 NBTI Compact Model

Considering Hole Trapping and Interface-State Generation

4.1 Introduction

Although the hydrogen reaction-diffusion (RD) theory was widely accepted for a long time, numerous experimental results measured by advanced technologies have indicated that such reaction-diffusion (RD) model exists inevitable limit in describing the transient degradation and recovery characteristics of NBTI effect [4.1, 4.2]. In spite of the existence and reaction of Si-H bonds at the interface of Si/SiO₂, which was demonstrated by experimental observations [4.3, 4.4], whether hydrogen- diffusion is essentially responsible for the long term degradation is still under discussion. Therefore, the origin of the NBTI degradation in p-MOSFET is required to be reconsidered. Recently, interface-state generation and hole-trapping in the gate oxide are considered as mechanisms of NBTI degradation. Whether these two mechanisms are independent or coupled is still open for discussion. Grasser et al. proposed that both mechanisms are tightly coupled. Such conclusion comes from the observation that the stress/recovery measurement results under different conditions are able to be scaled to a single universal curve, as shown in Fig. 4.1.1 (a) and (b) [4.5]. However such unified characteristic is not suit to the long term stress region and recovery period (Fig. 4.1.1 (c)), indicating that the independence of interface state generation and hole-trapping becomes obvious in the long term stress period and in the recovery process.

The independence of the interface state and hole-trapping mechanisms are further demonstrated by Huard et al. reported that the interface trap creation and hole-trapping/detrapping are independent mechanisms, and result in the permanent and recoverable degradation [4.6]. The normalized degradation under various temperature and bias conditions are shown in Fig. 4.1.2. In the short term region, the recoverable component dominates the degradation, while in the long term region, the permanent component starts

getting important.

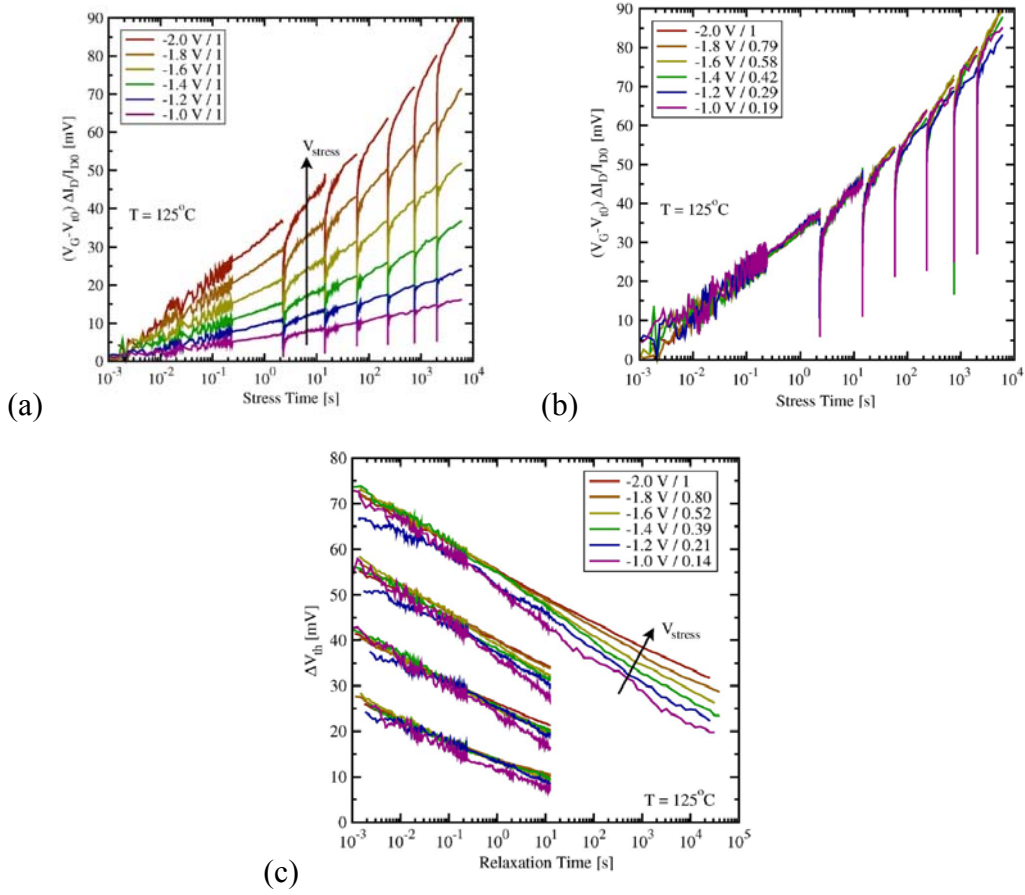


Fig. 4.1.1. (a) Measurement sequence for different stress voltages at $T = 125^\circ\text{C}$. (b) Scaled data with different scaling factors. In the long term region, the scaling curves show slight deviations. (c) Recovery data scaled to the first recovery point. No uniform characteristic can be observed.

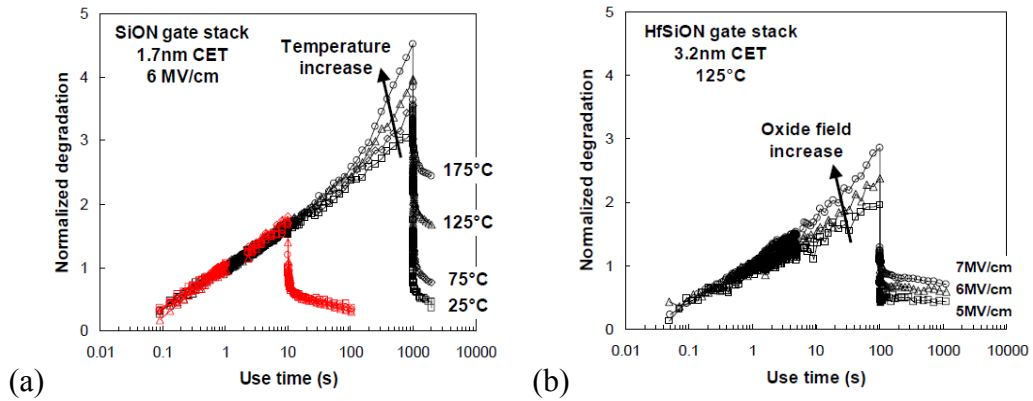


Fig. 4.1.2. (a) NBTI stress/recovery characteristics for 1.7nm SiON PNO gate stacks with temperature ranging from 25°C to 175°C . Recoverable component dominates the degradation in the short term region (red symbols) and permanent component dominates in the long term region. (b) NBTI stress/recovery characteristics for 3.2nm HfSiON gate stacks for various oxide fields.

In this chapter, the compact NBTI model considers both the hole-trapping and the

interface-state-generation as independent mechanisms, which enables a consistent prediction of the NBTI degradation for various conditions of stress biases, fabrication-process technologies, and frequencies. Except for bias dependence, the NBTI effect has been demonstrated featuring highly temperature sensitivity [4.7, 4.8]. The simulation with the hypothesis of constant temperature is possible to result in more than 50% simulation error compared to the results obtained by considering temperature variation [4.8]. Therefore, it is necessary to verify the NBTI predictive model under real circuit operation conditions.

4.2 Model Development

Hole-trapping and the interface-state generation have been widely accepted as two major mechanisms responsible for the NBTI degradation [4.9, 4.10]. The schematic view for the mechanisms is shown in Fig. 4.2.1.

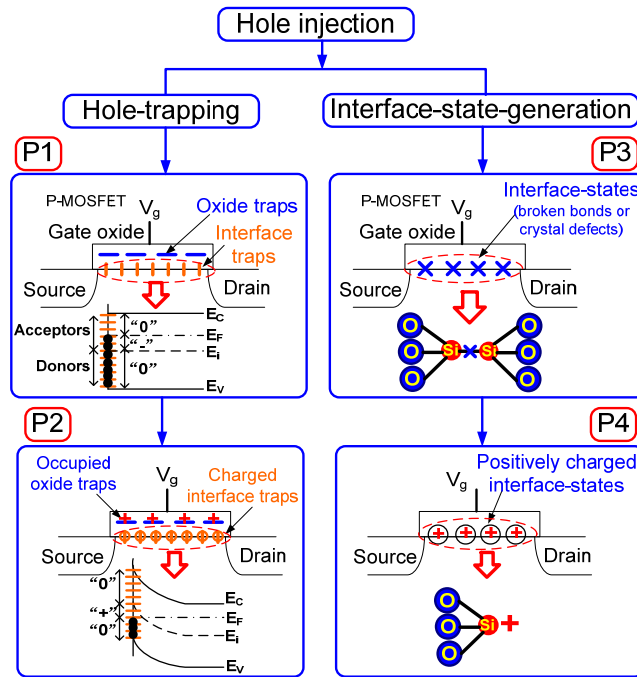


Fig. 4.2.1. Schematic view of hole-trapping and interface-state generation mechanisms.

There are two kinds of traps expected in a p-MOSFET (P1). One is defined as interface traps located at the interface. The other kind of traps is located within the gate oxide. Under negative gate bias, holes tunnel into the gate oxide have an opportunity to be captured by the

interface traps as well as the oxide traps (P2). At the same time, holes with high energy may generate interface-states by breaking chemical bonds (P3) [4.11, 4.12]. When holes are trapped by such defects, the interface-states are positively charged (P4) and cause the parallel shift of the flat-band voltage.

4.2.1 Hole-Trapping Model

Modeling for the hole-trapping in the existing states and gate oxide has been introduced in Chapter 3. For simplifying the structure of the thesis, only significant results are shown here.

The hole-trapping density is derived by solving Eq. (4.2.1) as

$$n_{T_int}(t) = N_{trap0} [1 - \exp(-kt)] = N_{trap0} [1 - \exp(-t / \tau_c)] \quad (4.2.1)$$

Here N_{trap0} is the density of trap sites existing at the interface. n_{T_int} is the density of trapped holes and k is the hole-trapping rate. t is the stress duration. $\tau_c = 1/k$ is defined as the hole-capture time.

Thus the density of holes trapped in the oxide (n_{T_ox}) is derived as

$$n_{T_ox} \approx \frac{N_0}{\lambda} \left(\frac{t}{\tau_0} \right)^{0.14} \quad (4.2.2)$$

Here $\tau_0 = 3e-4s$ is the trap generation time constant, $\lambda = 2nm^{-1}$ is the attenuation coefficient in the oxide. The threshold voltage degradation induced by hole-trapping mechanism ($\Delta V_{th_trap}^S$) is derived as

$$\Delta V_{th_trap}^S = \frac{q}{C_{ox}} (n_{T_int} + n_{T_ox}) \approx \frac{q}{C_{ox}} \left\{ N_{trap0} \left[1 - \exp\left(-\frac{t}{\tau_c}\right) \right] + \frac{N_0}{\lambda} \left(\frac{t}{\tau_0} \right)^{0.14} \right\} \quad (4.2.3)$$

After the stress is removed, ΔV_{th} recovers following an inverse process of the hole-trapping

$$\Delta V_{th_trap}^R = \Delta V_{th_trap}^{\max} \exp(-t / \tau_e) \quad (4.2.4)$$

Here τ_e is the hole-emission time constant. $\Delta V_{th_trap}^{\max}$ is the maximum ΔV_{th} at the end of the stress process.

4.2.2 Interface-State-Generation Model

Under high negative stress, holes with high energy have a possibility to create interface-states by breaking chemical bonds [4.12]. Investigation results from numerous literature reports based on measurements have demonstrated that the interface-state generation rate can be written as an exponential function of the gate oxide electric field (E_{ox}) [4.13, 4.14]

$$\frac{dn_{S_int}}{dt} = A \exp(BE_{ox}) \quad (4.2.5)$$

Here n_{S_int} is the density of generated interface-state. A and B are fitting parameters determined by applied materials and fabrication processes, where A is related to the oxide electric field due to the mobile carriers [4.1] and B reflects the E_{ox} sensitivity of interface-state generation. Considering the impact of generated interface state (n_{S_int}), E_{ox} is re-calculated as

$$\begin{aligned} E_{ox} &= \frac{V_g - V_{fb} - \varphi_s}{T_{ox}} = \frac{V_g - (V_{fb0} + \Delta V_{fb}) - \varphi_s}{T_{ox}} \\ &= \frac{V_g - V_{fb0} - \varphi_s}{T_{ox}} - \frac{\Delta V_{fb}}{T_{ox}} = E_{ox0} - \frac{qn_{S_int}}{C_{ox} T_{ox}} \end{aligned} \quad (4.2.6)$$

Here V_g is the applied gate bias. φ_s is the surface potential. ΔV_{fb} is the flat-band voltage shift, which is equivalent to ΔV_{th} . V_{fb0} and E_{ox0} are the flat-band voltage and the gate oxide field without degradation. T_{ox} is the thickness of the gate oxide. C_{ox} is the gate capacitance, and q is the electron charge. Substituting Eq. (4.2.6) into Eq. (4.2.5) result in

$$\frac{dn_{S_int}}{dt} = A \exp(BE_{ox}) = A \exp\left(BE_{ox0} - \frac{Bq}{C_{ox} T_{ox}} n_{S_int}\right) \quad (4.2.7)$$

Solving Eq. (4.2.7) and considering the boundary condition that $n_{S_int}=0$ at $t=0$, the generated interface-state density is written as

$$n_{S_int} = \frac{C_{ox} T_{ox}}{Bq} \log \left[1 + \frac{ABq}{C_{ox} T_{ox}} \cdot \exp(BE_{ox0}) \cdot t \right] \quad (4.2.8)$$

Since that only positively charged interface-states have the contribution to ΔV_{fb} , the hole occupation probability R_{S_int} is introduced as an exponential function of gate oxide electric field ($R_{S_int} \sim \exp(E_{ox0})$) [4.1], which is determined by the hole tunneling probability from substrate into the oxide as well as the reaction rate of the dangling band. Therefore, the

threshold voltage shift caused by interface-state generation during the stress process ($\Delta V_{th_int}^S$) is thus written as

$$\begin{aligned}\Delta V_{th_int}^S(t) &= \frac{q}{C_{ox}} \cdot (R_{S_int} \cdot n_{S_int}) = \frac{q}{C_{ox}} \cdot R_{S_int} \cdot \frac{C_{ox} T_{ox}}{Bq} \log \left[1 + \frac{ABq}{C_{ox} T_{ox}} \cdot \exp(BE_{ox0}) \cdot t \right] \\ &= \frac{q}{C_{ox}} \cdot R_{Eox} \log \left(1 + \frac{t}{\tau_S} \right)\end{aligned}\quad (4.2.9)$$

$$\tau_S = \frac{C_{ox} T_{ox}}{ABq \cdot \exp(BE_{ox0})} \quad \text{and} \quad R_{Eox} = \frac{R_{S_int} C_{ox} T_{ox}}{Bq} \quad (4.2.10)$$

Here τ_S is defined as the interface-state generation time constant, indicating the shortest time required for the interface-state generation, which is insensitive to the bias condition but determined by the applied materials and the manufacturing process [4.15, 4.16]. R_{Eox} is defined as the generation rate of interface-states.

After the stress is removed, holes captured by the interface-states are released and re-enter into the silicon substrate, reducing the density of the positively charged interface-state. ΔV_{th} recovery ($\Delta V_{th_int}^R$) is modeled as an inverse process of interface-state generation

$$\Delta V_{th_int}^R(t) = \Delta V_{th_int}^{\max} - \Delta V_{th_int}^{\max} \cdot R_{rec} \log \left(1 + \frac{t}{\tau_{rec}} \right) \quad (4.2.11)$$

Here $\Delta V_{th_int}^{\max}$ is the maximum ΔV_{th} at the end of the stress, and decreases continuously during the procedure of recovery. R_{rec} is the recovery rate coefficient. τ_{rec} is the time constant for recovery or healing of interface-states generated during the previous stress process.

The unified compact prediction model is finally developed by combining both mechanisms of hole-trapping and interface- state generation

$$\Delta V_{th} = \Delta V_{th_trap} + \Delta V_{th_int} \quad (4.2.12)$$

4.3 Model Verification

4.3.1 Model Verification for DC Bias Conditions

The unified NBTI model is verified using the experimental data from different literatures. The model parameters are listed in Table. 4.3.1, and the values are extracted from the measured data [4.17, 4.18].

Table. 4.3.1. Model parameters of the compact NBTI model

Parameter	Definition	Value
τ_0 [s] ^{a)}	trap generation time constant	3e-4
τ_S [s] ^{a)}	Interface state generation time constant	5e-4
τ_{rec} [s] ^{a)}	Interface state recovery time constant	5e-7
τ_c [s] ^{b)}	Hole capture time constant	Fig. 4.3.2(a)
τ_e [s] ^{b)}	Hole emission time constant	$\tau_e = \tau_c$
R_{Eox} ^{b)}	Interface state reaction rate coefficient	Fig. 4.3.2(a)
N_0 [cm ⁻³] ^{b)}	Gate oxide trap density close to the interface	Fig. 4.3.2(b)
N_{trap0} [cm ⁻²] ^{b)}	Interface trap density	Fig. 4.3.2(b)
R_{rec} ^{b)}	Interface state recovery rate coefficient	Fig. 4.3.5

a) Physical parameter

b) Fitting parameter

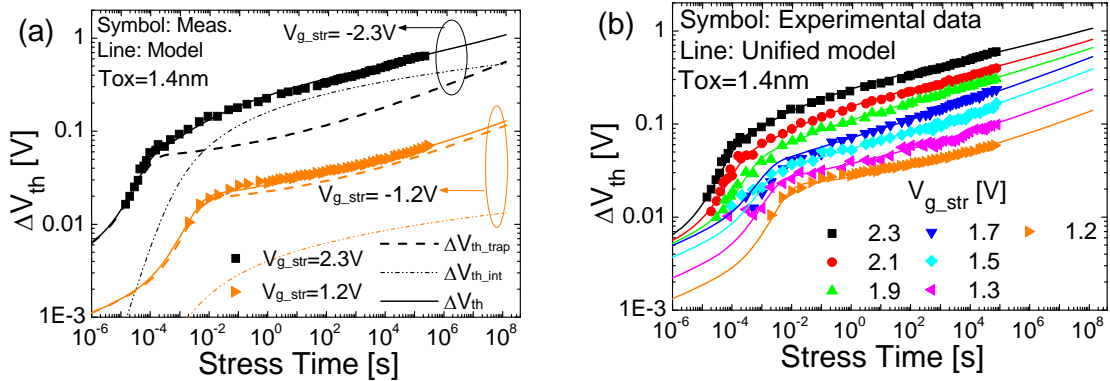


Fig. 4.3.1. (a) Separated effects of hole-trapping and interface-state generation to the V_{th} shift with stress biases $V_{g_str} = -2.3$ and $-1.2V$. (b) Unified NBTI model results compared with measured data [4.17].

In order to have a clear view of the contributions of interface-state generation and hole-trapping to the V_{th} degradation, ΔV_{th} at stress biases of $V_{g_str} = -2.3V$ and $-1.2V$ are separated into components of interface-state generation and hole-trapping, as shown in Fig. 4.3.1(a). Under high stress bias ($V_{g_str} = -2.3V$), the hole-trapping mechanism dominates the ΔV_{th} in the short term region. While the interface-state generation induced degradation (ΔV_{th_int}) is much larger than that of the hole-trapping (ΔV_{th_trap}) for the long term stress. With V_{g_str} decreased to $-1.3V$, ΔV_{th_trap} is observed decreasing much slower than ΔV_{th_int} and

hole-trapping dominates ΔV_{th} even in the long term region. By combining both mechanisms of the hole-trapping and interface-state generation, the compact NBTI model shows a good agreement with measurement over a wide range of stress time duration under various stress bias condition ranging from -1.2V to -2.3V [4.17], as shown in Fig. 4.3.1(b).

The stress bias condition dependence of the interface-state generation rate coefficient (R_{Eox}), hole-capture time constant (τ_c), hole density injected into gate oxide from substrate (N_0) and existing trap density (N_{trap0}) extracted from Fig. 4.3.1 are summarized in Fig. 4.3.2. R_{Eox} increases following an exponential function of V_{g_str} (equivalent to E_{ox}), which is consistent with the derivation of Eq. (4.2.9). Moreover, the decreased τ_c (in Fig. 4.3.2(a)) and increased N_{trap0} (in Fig. 4.3.2(b)) indicates that higher V_{g_str} increases the hole-trapping probability at the deep trap levels as well as the available trap density [4.19]. The hole density injected into the gate oxide (N_0) is relative to the gate leakage current ($N_0 \sim J_g \sim \exp(-1/V_{g_str})$) [4.20, 4.21], which is also demonstrated from the parameter extraction in Fig. 4.3.2(b).

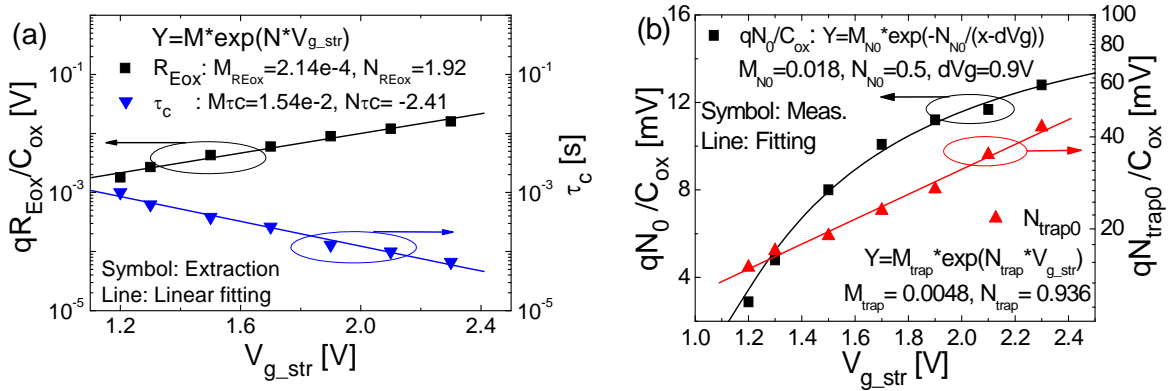


Fig. 4.3.2. (a) Extracted stress bias condition dependence of the interface-state generation rate coefficient (R_{Eox}) and hole capture time constant (τ_c). Here M and N are fitting parameters. (b) Available trap site density (N_{trap0}) and density of holes injected into the gate oxide (N_0). Here N_0 is relative to the gate leakage current ($N_0 \sim J_g \sim \exp(-1/V_{g_str})$).

The compact NBTI model is capable to accurately describe also ΔV_{th} recovery characteristic [4.18]. Fig. 4.3.3(a) separates hole-detrapping (ΔV_{th_int}) and interface-state recovery (ΔV_{th_trap}). Since the measurements are carried out with high stress bias of $V_{g_str} = -2.8$ V, the interface-state generation dominates the degradation. Fig. 4.3.3 (b) shows the enlarged hole-detrapping characteristic, which recovers fast in the initial stage. Fig. 4.3.4 (a) and (b) compare the model results with measurements [4.18] in semi-logarithmic and linear scale, respectively. Good agreement is observed. The recovery rate coefficient R_{rec} extracted

from measurement data (Fig. 4.3.4) is observed sensitive to the time duration of the previous stress process, as plotted in Fig. 4.3.5. A reduction of R_{rec} with increased stress time maybe possibly due to the deep level traps with larger hole-emission time constant [4.22].

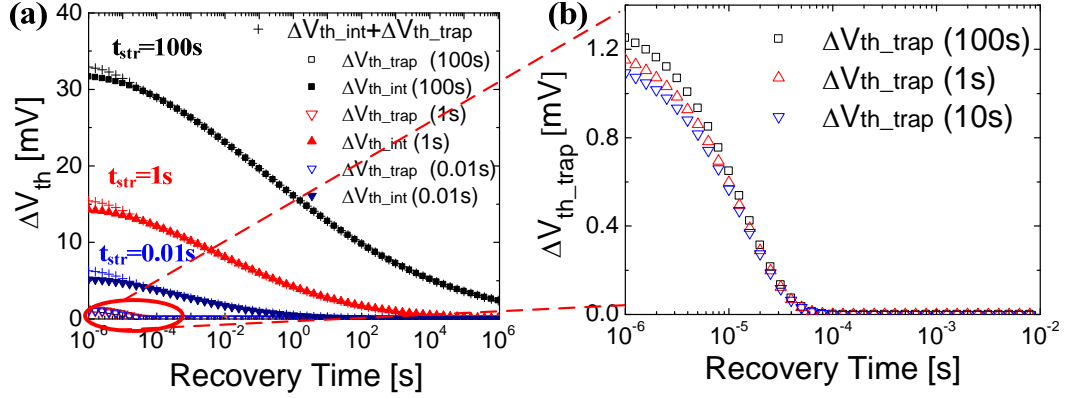


Fig. 4.3.3. (a) Separated recovery characteristics of interface-state generation and hole-trapping. (b) Enlarged characteristic of the hole-detraping process.

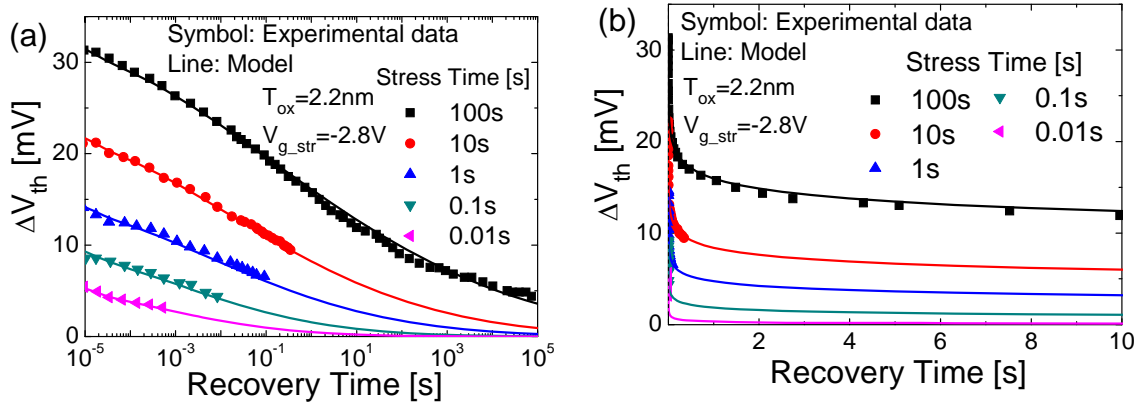


Fig. 4.3.4. (a) ΔV_{th} recovery characteristics plotted in semi-log scale and (b) linear scale. Data is from [4.18].

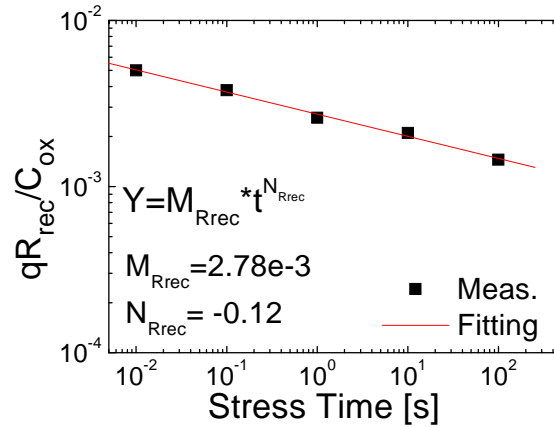


Fig. 4.3.5. Stress time dependence of the recovery rate coefficient R_{rec} .

4.3.2 Model Verification for AC Bias Conditions

The cycle-to-cycle dynamic NBTI effect is modeled based on the static model developed above. The ΔV_{th} during several stress/recovery cycles are able to be reproduced using the dynamic NBTI model summarized in Table. 4.3.2.

Table. 4.3.2. Dynamic NBTI model development.

Dynamic NBTI Model (here i is the cycle number)	
Stress	
Interface	$\Delta V_{th_trap, i}^S = \Delta V_{th_trap}^{\min}(t_{S, i-1}) + \frac{qN_{trap0}}{C_{ox}} \left[1 - \exp\left(-\frac{t_{S, i}}{\tau_c}\right) \right] \quad (4.3.1)$
Hole-Trapping	$\Delta V_{th_trap, i}^{\max} = \Delta V_{th_trap, i}^S \Big _{t=t_{S, i}} \quad (4.3.2)$
Oxide Hole-Trapping	$V_{th_ox, i}^S = \frac{q}{C_{ox}} \cdot \frac{N_0}{\lambda} \left(\frac{\sum_{i=1}^{N_{CLK}} t_{S, i}}{\tau_0} \right)^{0.14} \quad (4.3.3)$
	$\Delta V_{th_ox, i}^{\max} = \Delta V_{th_ox, i}^S \Big _{t=t_{S, i}} \quad (4.3.4)$
	$\Delta V_{th_int, i}^S = \Delta V_{th_int, i-1}^{\min} + \Delta V_{th_int, i-1}^{\min} \cdot R_{Eox} \log\left(1 + \frac{t_{S, i}}{\tau_s}\right) \quad (4.3.5)$
Interface-state generation	$\Delta V_{th_int, i}^{\max} = \Delta V_{th_int, i}^S \Big _{t=t_{S, i}} \quad (4.3.6)$
ΔV_{fb} during stress	$\Delta V_{th, i}^S = \Delta V_{th_trap, i}^S + \Delta V_{th_ox, i}^S + \Delta V_{th_int, i}^S \quad (4.3.7)$
Recovery	
Interface	$\Delta V_{th_trap, i}^R = \Delta V_{th_trap, i-1}^{\max} \exp(-t_{R, i} / \tau_e) \quad (4.3.8)$
Hole-Trapping	$\Delta V_{th_trap, i}^{\min} = \Delta V_{th_trap, i}^R \Big _{t=t_{R, i}} \quad (4.3.9)$
Oxide Hole-Trapping	$\Delta V_{th_ox, i}^R = \Delta V_{th_ox, i}^{\max} \quad (4.3.10)$
	$\Delta V_{th_int, i}^R = \Delta V_{th_int, i-1}^{\max} - \Delta V_{th_int, i-1}^{\max} \cdot R_{rec} \log\left(1 + \frac{t_{R, i}}{\tau_{rec}}\right) \quad (4.3.11)$
Interface-state generation	$\Delta V_{th_int, i}^{\min} = \Delta V_{th_int, i}^R \Big _{t=t_{R, i}} \quad (4.3.12)$
ΔV_{fb} during recovery	$\Delta V_{th, i}^R = \Delta V_{th_trap, i}^R + \Delta V_{th_ox, i}^R + \Delta V_{th_int, i}^R \quad (4.3.13)$

In Table. 4.3.2, $\Delta V_{th_trap, i}^S$, $\Delta V_{th_ox, i}^S$ and $\Delta V_{th_int, i}^S$ are threshold shift induced by hole-trapping at the interface, within the gate oxide, and interface-state generation in the i^{th} duty cycle, respectively. $\Delta V_{th_trap, i}^R$, $\Delta V_{th_ox, i}^R$ and $\Delta V_{th_int, i}^R$ indicate the recovery of these three components. $\Delta V_{th, i}^S$ and $\Delta V_{th, i}^R$ indicate the final result of the V_{th} shift during the i^{th} stress/recovery and used for next step calculation. $t_{S, i}$ and $t_{R, i}$ are stress and recovery time of the i^{th} duty cycle. N_{CLK} is the number of the stress/recovery cycle. Since the hole-trapping within the gate oxide is assumed unrecoverable even without stress bias, the ΔV_{th} induced by oxide traps features an accumulation effect of the stress time, and keeps constant during the recovery process.

Fig. 4.3.6(a)-(c) show the comparison between the dynamic NBTI model and measured data with duty cycle of 3%, 50% and 97%, respectively [4.23]. The stress bias $V_{g_str}=-1.8V$ and recovers to 0V. The stress/recovery cycle time is $T_{CLK}=1000s$. The model results show good agreement with the measured data even during several stress/recovery cycles.

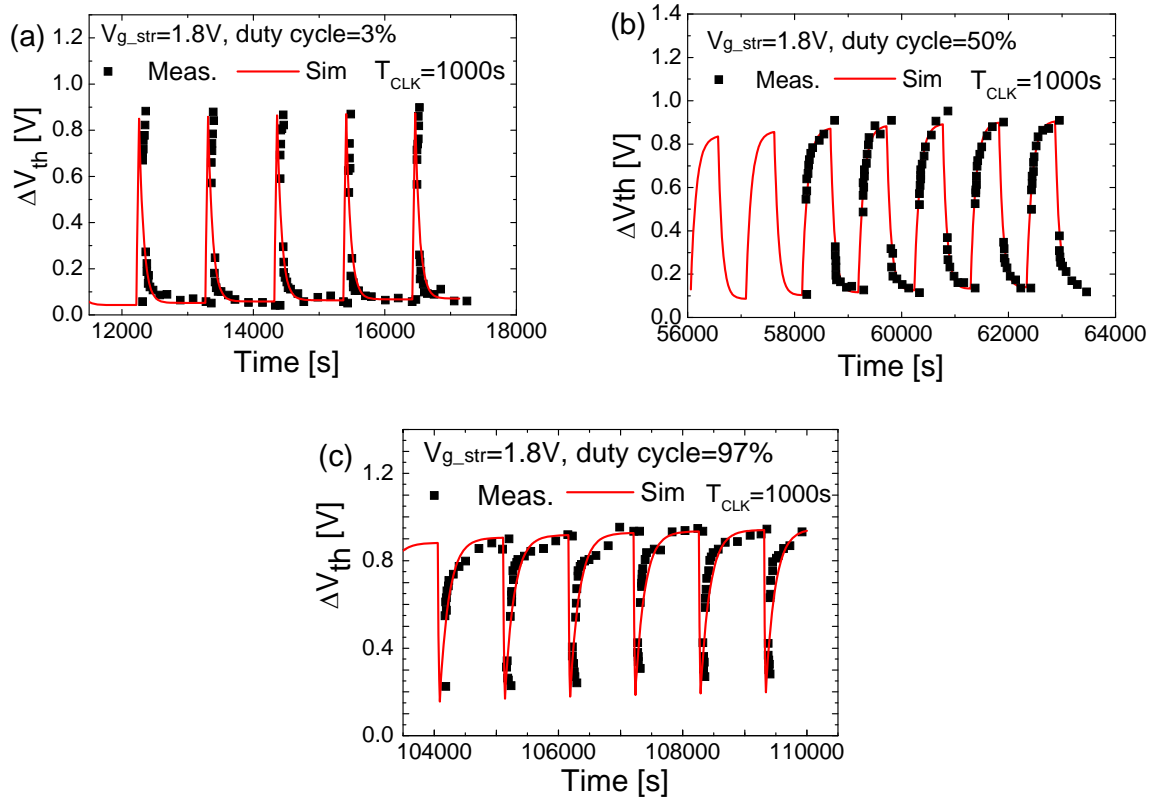


Fig. 4.3.6. Verification of the developed predictive model using measured data with stress bias of -1.8V, recovery bias of 0V, stress/recovery cycle time $T_{CLK}=1000s$, duty cycle of (a) 3%, (b) 50% and (c) 97% (data is from [4.30]).

The long term degradation with cycle time of $T_{CLK}=1000s$ is shown in Fig. 4.3.7. The maximum and minimum ΔV_{th} bounds are extracted from measured data. The simulation result of the dynamic NBTI effect fits well with the measured data.

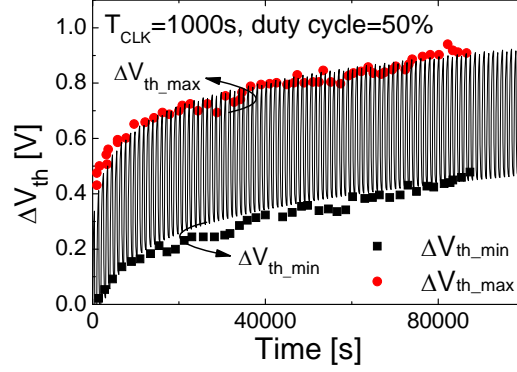


Fig. 4.3.7. The long term degradation under AC stress condition with stress/recovery cycle time $T_{CLK}=1000s$ (data is from [4.23]).

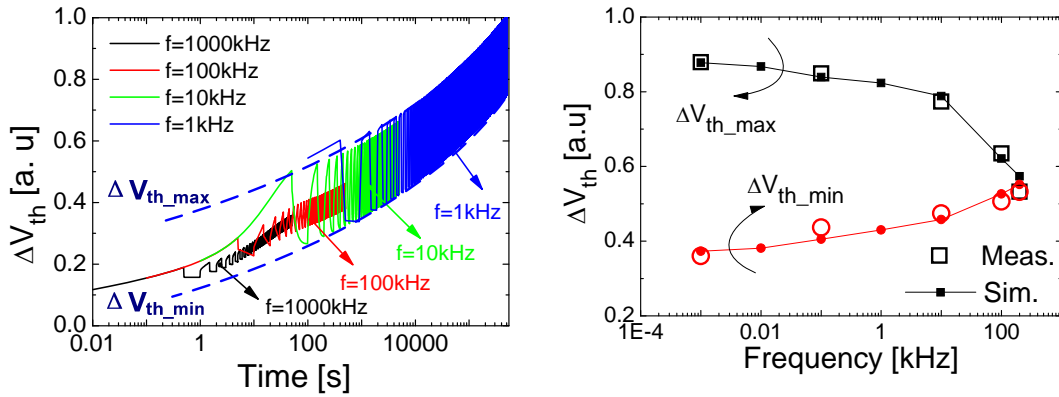


Fig. 4.3.8. (a) Simulation result of AC NBTI degradation with various frequencies. (b) Frequency dependence of ΔV_{th_max} and ΔV_{th_min} for p-MOSFET samples with DPN SiON of 1.3nm EOT with stress bias $V_{g_str}=-2.4V$ [4.4].

Under the AC stress, the ΔV_{th} is characterized by two specific values: the maximum value (ΔV_{th_max}) and the minimum value (ΔV_{th_min}) observed during each stress-recovery cycle (defined in Fig. 4.3.7). The AC NBTI degradation for various frequencies is simulated in Fig. 4.3.8. As shown in Fig. 4.3.8(a), the amplitude between ΔV_{th_max} and ΔV_{th_min} increases with reduced frequency (increased cycle time). Such phenomenon is mainly because that the increased frequency reduces the stress and recovery time during each stress/recovery cycle. For ultra high frequency, the holes injected into the gate oxide do not have enough time to be trapped or released by the defects, thus the difference between ΔV_{th_max} and ΔV_{th_min} almost

reduces to zero. The frequency dependence of ΔV_{th_max} and ΔV_{th_min} are extracted in Fig. 4.3.8(b). The modeling result shows a good agreement with the measured data [4.2].

The duty cycle dependence of ΔV_{th_max} features a standard “S-shape” curve with the duty cycle ranging from 1% to 99%, as shown in Fig. 4.3.9. The “S-curves” with duty time of $T_{CLK}=1000s$, 500s and 100s are simulated. Among them, the simulation result with $T_{CLK}=1000s$ is consistent with the previous reports [4.23].

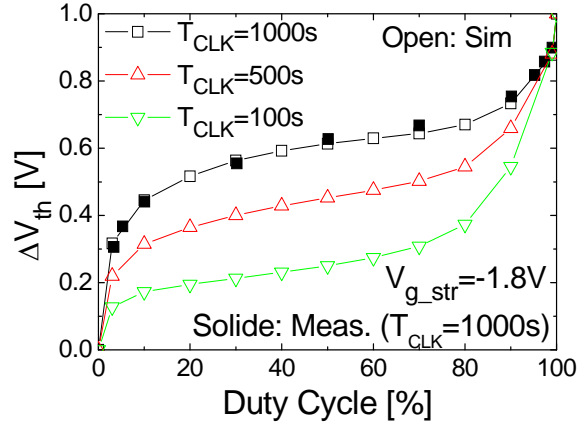


Fig. 4.3.9. Verification of the developed model with the typical “S-shape” duty cycle dependence (data is from [4.23]).

4.3.3 Model Verification for Different Technologies

The developed unified NBTI model is also capable to explain another series of measured data with different technologies [4.17], as shown in Fig. 4.3.10. S1 is a high-K gate dielectric, S2 a thermally nitrided dielectric with the highest nitrogen density, S3 a plasma treated dielectric with the lowest nitrogen density, S4 and S5 are plasma treated dielectrics with the same nitrogen density for 45s and 20s, respectively. The extracted model parameters are summarized in Table 4.3.3.

For the same technology (S4 & S5), longer plasma treated time (45s) results in higher interface trap density (qN_{trap0}/C_{ox}) with larger capture time constant (τ_c), indicating that increased numbers of deep level traps are generated. The sample with high-K gate dielectrics (S1) features highest interface trap density (qN_{trap0}/C_{ox}), highest gate oxide trap density (qN_0/C_{ox}), as well as highest interface-state generation probability (qR_{Eox}/C_{ox}).

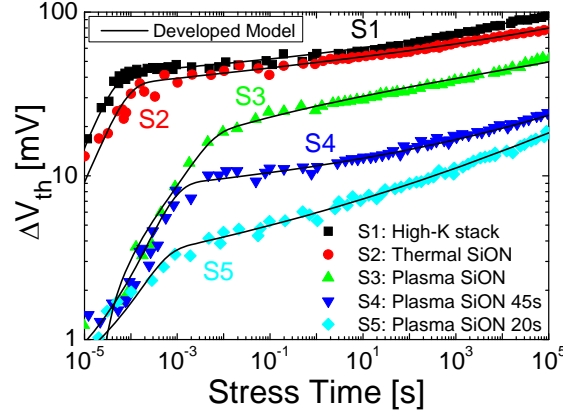


Fig. 4.3.10. NBTI degradation in samples fabricated with different technologies and different bias conditions [4.24].

Table. 4.3.3. Technology and model parameters extracted from Fig. 4.3.10.

Parameter	S1	S2	S3	S4	S5
T_{ox} (nm)	3.0	2.7	1.4	2	2
V_{g_str} (V)	1.2	1.5	1.2	1.2	1.2
E_{ox} (MV/cm)	4	5.6	8.6	6	6
qR_{Eox}/C_{ox}	7e-4	1e-3	1.5e-3	1.4e-4	8e-5
qN_{trap0}/C_{ox}	3.7e-2	3e-2	9e-3	7e-3	2e-3
qN_0/C_{ox}	9e-2	5e-2	1.5e-2	2.7e-2	3e-2
τ_s	1e-6	1e-6	1e-6	1e-6	1e-6
τ_c	2.9e-5	5.3e-5	3.3e-3	5.9e-4	3e-4

4.3.4 Model Verification from Temperature-Dependence Point of View

The temperature dependence of parameters in interface- state generation model and hole-trapping model are derived in Table 4.3.4. The exponentially temperature dependence of hole- emission time constant (τ_e) of the interface defect has been demonstrated by theory analysis and experimental results (Eq. (4.3.14)) [4.24, 4.25]. The hole-injection density (N_0) into the gate oxide is proposed relative to the gate current. Although the gate tunneling current

is known to be insensitive to the temperature in ideal MOSFET, the impact of oxide traps on gate current should not be neglected. Since the hole-occupation probability (f_{FD}) of the defects are determined by the Fermi-Dirac statistic distribution, which is function of temperature (Eq. (4.3.15)) [4.26], the trap assistant gate leakage current is responsible for the temperature dependence of injected hole density.

Table. 4.3.4. Temperature dependence of the NBTI model parameters

Hole-emission time constant (Eq. 4.2.4)		
$\tau_e = [\nu_{th} N_c \sigma_n \exp(-\Delta E_t / k_B T)]^{-1} \propto \exp(\Delta E_t / k_B T)$		(4.3.14)
Oxide trap density close to the Si/SiO₂ interface (Eq. 4.2.2)		
$f_{FD} = \frac{1}{1 + \exp\left[\frac{q(\varphi_B - \varphi)}{k_B T}\right]} \Rightarrow N_0 \propto \exp\left[-\frac{q(\varphi_B - \varphi)}{k_B T}\right]$		(4.3.15)
Interface trap generation model (Eq. 4.2.9)		
$k_f \propto \exp(-E_a / k_B T) \cdot \exp[(\gamma_{T0} / k_B T) E_{ox}]$		(4.3.16a)
$\frac{dn_{S_{int}}}{dt} = A \exp(BE_{ox})$		(4.2.5)
$\Rightarrow A \propto \exp(-E_a / k_B T) \quad \& \quad B \propto \gamma_{T0} / (k_B T) \quad \& \quad \text{Eq. 11}$		(4.3.16b)
$\Rightarrow \begin{cases} R_{Eox} = C_{ox} T_{ox} / (Bq) \propto (1 / k_B T)^{-1} \end{cases}$		(4.3.16c)
$\Rightarrow \begin{cases} \tau_S = C_{ox} T_{ox} / [A \cdot Bq \cdot \exp(BE_{ox0})] \propto \exp(1 / k_B T) \end{cases}$		(4.3.16d)
v_{th}	Carrier thermal velocity	Intermediate variables Ref. [4.4, 4.6]
N_c	Effective state density in the conduction band	
σ_n	capture cross section	
E_a	Si bond dissociation active energy	
γ	field acceleration parameter	
$q(\varphi_B - \varphi)$	Trap energy level	
ΔE_t	Hole-emission active energy	

For the interface-state generation mechanism, the temperature dependence of the forward generation rate (k_f) has been developed in ref [4.1] (Eq. (4.3.16a)). Comparing with the

interface-state generation equation (Eq. (4.2.5)), the coefficients A and B are derived, as shown in Eq. (4.3.16b). Combining with the simplified expression (Eq. 4.2.9), the temperature dependence of the interface-state generation rate (R_{Eox}) and time constant (τ_s) are calculated in Eq. (4.3.16c) and Eq. (4.3.16d), respectively. The above hypothesis is validated using the measurement results at various temperatures under stress and recovery conditions. Model parameters extracted from data-fitting are listed in Table. 4.3.3, as well as plotted in Fig. 4.3.11 and Fig. 4.3.12.

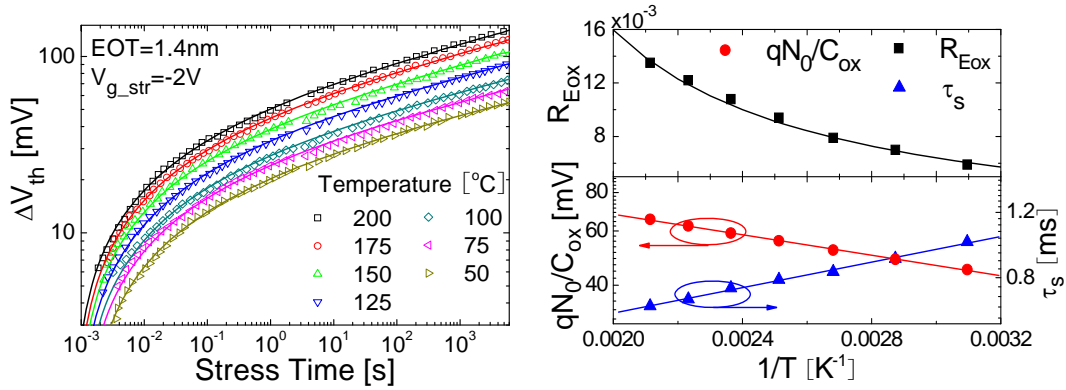


Fig. 4.3.11. (a) Temperature dependence of ΔV_{th} under stress condition [4.5]. (b) The temperature dependence of generation rate ($R_{\text{Eox}} \sim (1/T)^{-1}$), hole-injection density ($N_0 \sim \exp(-1/T)$), interface-state generation time constant ($\tau_s \sim \exp(1/T)$) and. The extraction results are consistent with Eqs. 4.3.16d, Eq. 4.3.16e and Eq. 4.3.15.

Fig. 4.3.11 (a) compares the measurement and model results of ΔV_{th} with temperature changing from 50°C to 200°C [4.5]. The model parameters of hole-injection density (N_0), interface-state generation rate (R_{Eox}) and the time constant (τ_s) are extracted by fitting the measured data. The temperature dependence of the parameters are plotted in Fig. 4.3.11(b), which are consistent with the speculations in Eq. 4.3.15, Eq. 4.3.16d and Eq. 4.3.16e.

Fig. 4.3.12(a) shows the ΔV_{th} recovery with temperature ranging from -40°C to 125°C [4.27]. Both the hole-emission time constant (τ_e) and recovery time constant (τ_{rec}) increase exponentially with increased temperature, indicating that the recovery procedure slows down with decreased temperature (Fig. 4.3.12(b)). Moreover, compared to τ_{rec} , τ_e features a faster increase characteristic with decreased temperature (increased $1/T$). The hole emission time constant ($\tau_e \sim \exp(1/T)$), interface state recovery rate ($\tau_{\text{rec}} \sim \exp(1/T)$) and recovery time constant ($R_{\text{rec}} \sim (1/T)^{-1}$) are consistent with the results obtained under stress conditions (Fig. 4.3.11(b)).

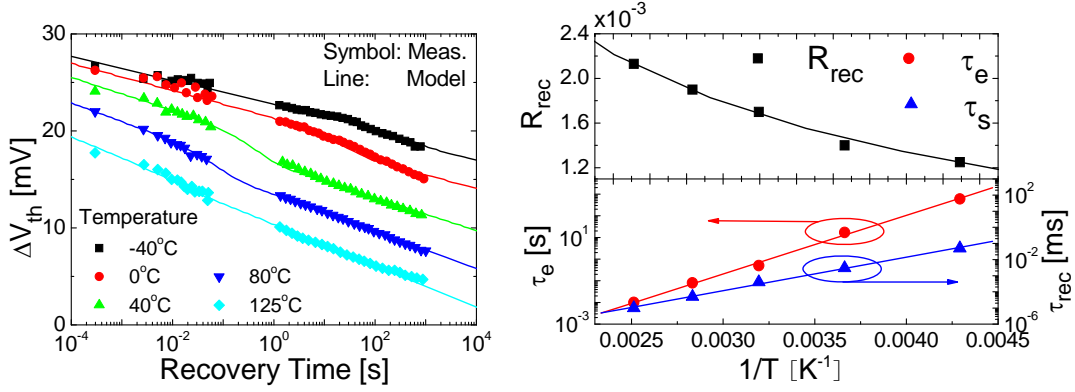


Fig. 4.3.12. Temperature dependence of (a) ΔV_{th} recovery [4.27] and (b) Hole emission time constant (τ_e), interface state recovery rate (R_{rec}) and time constant (τ_{rec}). The results are consistent with stress process.

The developed model is also capable to simulate the transition of ΔV_{th} recovery characteristics between various temperatures, as shown in Fig. 4.3.13. A smooth transition is able to be accurately reproduced during both heating and cooling procedures [4.27, 4.28].

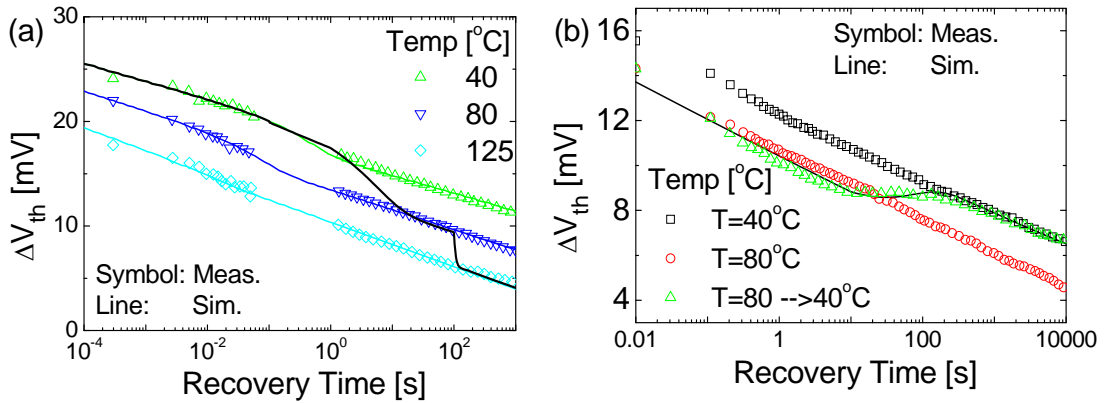


Fig. 4.3.13. Transition of recovery characteristics between various temperatures. (a) Temperature elevates from 40°C, 80°C to 125°C [4.27]. (b) Temperature is cooled down from 80°C to 40°C [4.28].

4.4 Hot Carrier Enhanced NBTI Model

In most experimental researches, the NBTI effect is studied under the worst degradation condition with gate stress bias only without the drain voltage. However, in some real circuits (e.g. amplifier and power switch) [4.29, 4.30], MOSFETs are usually operated with the applied drain bias (V_{ds}), which weakens the NBTI effect but enhances the channel hot carrier (CHC) effect [4.31, 4.32].

The origin of CHC and NBTI effects in p-MOSFET is illustrated in Fig. 4.4.1. In the real

circuits, p-MOSFETs are operated with the source bias (V_s) of the applied voltage V_{dd} , gate bias V_g and drain bias V_d . Surface potentials at source, pinch-off point, drain junction and drain are denoted by ϕ_{s0} , ϕ_{sL} , $\phi_{sL}(\Delta L)$ and $\phi_{s0}+V_{ds}$. Length of the pinch-off region is ΔL . With applied V_d , the vertical electric field in the gate oxide (E_{ox}) generally decreases from source to drain, thus weakens the pure NBTI effect by reducing the dissociation of Si bonds. Simultaneously, the lateral channel field increases and reaches a maximum value (E_{max}) close to the drain. Such peak field enhances the CHC effect by accelerating the channel carriers to form hot holes, which generate interface states at the interface of Si/SiO₂.

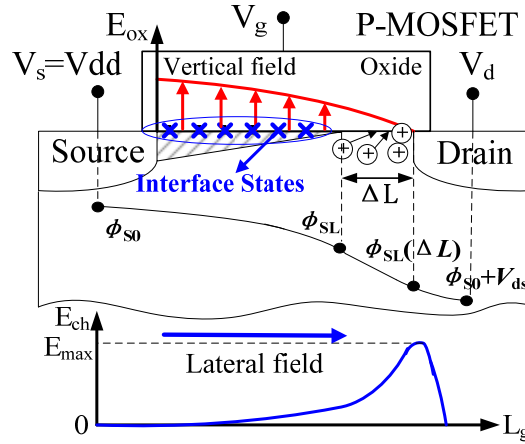


Fig. 4.4.1. Illustration of the CHC and the NBTI coupling effects. With the applied V_{ds} . The surface potentials at source, pinch-off point, drain junction and drain are ϕ_{s0} , ϕ_{sL} , $\phi_{sL}(\Delta L)$ and $\phi_{s0}+V_{ds}$. The pinch-off region length is ΔL .

When V_{ds} is applied to the drain, the lateral channel electric field is enhanced and reaches its maximum value (E_{max}) at the drain side. Such E_{max} accelerates the channel carriers into hot holes, which generate interface states close to the drain. The V_{th} degradation due to the CHC is modeled using the classical expression [4.33]

$$\Delta V_{th_CHC} = C \left\{ \exp[-\phi_{it} / (q\lambda E_{max})] \cdot (I_{ds} / W) \cdot t \right\}^m \quad (4.4.1)$$

Here C is a fitting parameter, which is expected to be insensitive to the bias conditions. ϕ_{it} is the critical energy for creating an interface trap, λ is the hot hole mean-free path, and E_{max} is the maximum lateral channel electric field, which is calculated using the compact model HiSIM. The drain current is defined by I_{ds} , W is the channel width, and m is extracted from experiments [4.33].

Combining with the NBTI model developed in Section 4.2, the final consistent model is written as

$$\Delta V_{th} = \Delta V_{th_NBTI} + \Delta V_{th_CHC} \quad (4.4.2)$$

Fig. 4.4.2 shows the implementation-flow chart of NBTI and CHC models into the surface-potential-based compact model HiSIM. In the NBTI model, the flat band voltage ($V_{fb,i}$) and the vertical gate oxide field ($E_{ox,i}$) at the i th time step (t_i) are first calculated with HiSIM ($E_{ox,i} = (V_g - V_{fb,i} - \phi_{s,i}) / T_{ox}$). Then NBTI induced ΔV_{th} [$\Delta V_{th_NBTI}(t_i)$] is obtained from Section 4.2. Then $\Delta V_{th_NBTI}(t_i)$ is added to $V_{fb,i}$ for the next-step calculation. In the CHC model, pinch-off-region length (ΔL), surface potentials at the source (ϕ_{s0}), drain junction [$\phi_s(\Delta L)$] and the pinch-off point (ϕ_{sL}) are obtained from HiSIM and used for calculating the maximum channel field E_{max} . With the calculated I_{ds} , the CHC induced ΔV_{th} [$\Delta V_{th_CHC}(t_i)$] is calculated. Model parameter values are listed in Table. 4.4.1.

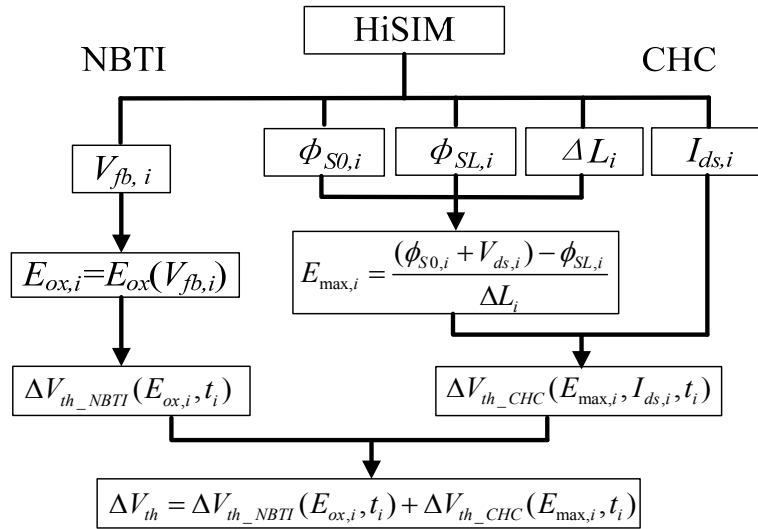


Fig. 4.4.2. Flow chart of NBTI and CHC models implementation into HiSIM model.

Table. 4.4.1. Model parameters of the CHC model

Parameter	Definition	Value
M	CHC degradation time exponent	0.5
C [V]	Constant relative to material and processes	0.05
ϕ_{it} [eV]	Critical energy for creating an interface trap	0.3
λ [s]	Hot hole mean-free path	1e-6

With increased V_{ds} , E_{ox} decreases along the channel direction from source to drain. Therefore, the dissociation of the interface silicon bond is weakened, which is reflected as the reduction of the pure NBTI effect, as shown in Fig. 4.4.3(a). Simultaneously, the lateral channel electric field is enhanced, and features a maximum channel field (E_{max}) close to the drain side, as shown in Fig. 4.4.3(b). The drain bias dependence of E_{max} is extracted in the insert figure.

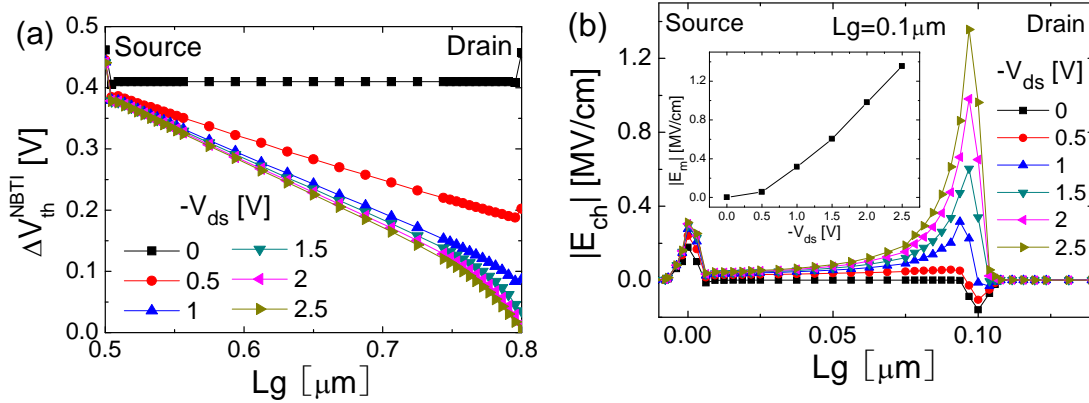


Fig. 4.4.3. (a) Calculation results of distribution of Vertical oxide field (E_{ox}) along the channel. (b) Lateral channel field (E_{ch}). Inset figure: V_{ds} dependence of the E_m .

Using the surface-potential-based compact model HiSIM, the maximum channel field E_{max} and drain current I_{ds} are calculated, as shown in Fig. 4.4.4(a) and (b).

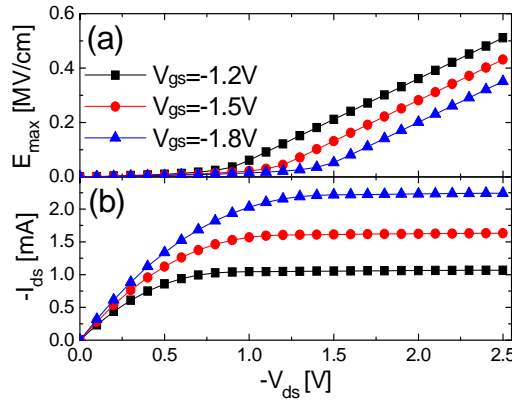


Fig. 4.4.4. (a) Maximum lateral channel field (E_{max}) and (b) drain current (I_{ds}) calculated using HiSIM.

With the calculated E_{max} and I_{ds} , the contribution of NBTI and CHC effects to ΔV_{th} are calculated as shown Fig. 4.4.5 separately and compared with the measurement data [4.31]. As investigate in section II, with increased V_{ds} , NBTI degradation is reduced and CHC degradation is enhanced. With gate bias V_{gs} increasing from -1.2V to -1.8V, both NBTI effect and CHC effect are increased. The consistent predictive model shows a good agreement with

the measured data.

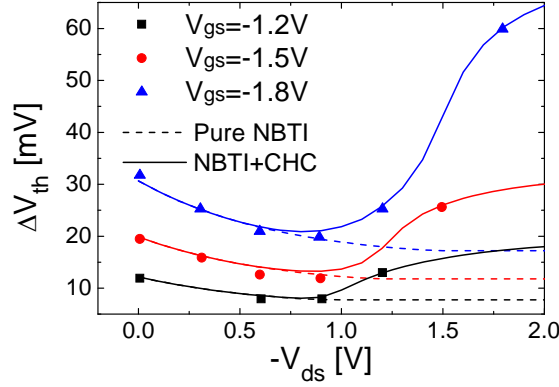


Fig. 4.4.5. V_{ds} dependence of ΔV_{th} induced by pure NBTI (dashed lines) and coupled effects with CHC (solid lines) under various V_{gs} . Good agreement is obtained when compared to the measured data [4.6].

The gate length dependence of the CHC effect is shown in Fig. 4.4.6(a) for channel length of $L_g=0.1$ and $0.3\mu\text{m}$ [4.30]. Since NBTI degradation is mainly due to the vertical electric field in the gate oxide, the NBTI effect does not show evident L_g dependence. In contrast, the CHC effect is obviously enhanced with scaled L_g due to the strong L_g dependence of E_{max} . Fig. 4.4.6(b) compares the model results with the measured data for various channel lengths. Good agreement is obtained.

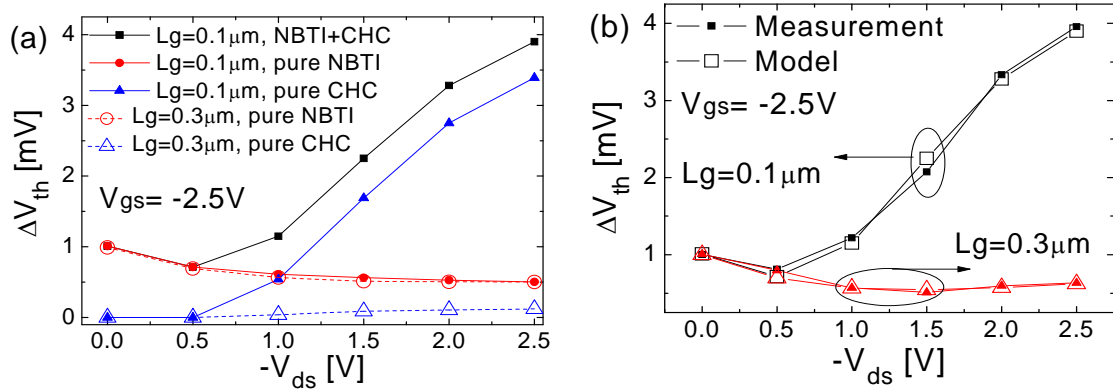


Fig. 4.4.6. (a) Calculation results of the separated and coupled contribution of NBTI and CHC to ΔV_{th} with $L_g=0.3$ and $0.1\mu\text{m}$ under $V_{gs} = V_{ds} = -2.5V$. (b) Comparison between model result and measurement [4.4].

With the model parameters extracted from the measured data as shown in Fig. 4.4.6, the

time dependence of ΔV_{th} is simulated under the conditions of $V_{gs} = -2.5V$ and various V_{ds} . Fig. 4.4.7(a) shows the separated contribution of the NBTI effect and the CHC effect over wide stress time duration. The CHC effect induces less degradation than NBTI effect under low V_{ds} , whereas ΔV_{th_CHC} increases with increased V_{ds} and even becomes comparable to ΔV_{th_NBTI} . Therefore, ΔV_{th} is enhanced by CHC especially in the long term region although the NBTI effect is suppressed, as shown in Fig. 4.4.7(b), which is consistent with the measurement reported in the previous works [4.34].

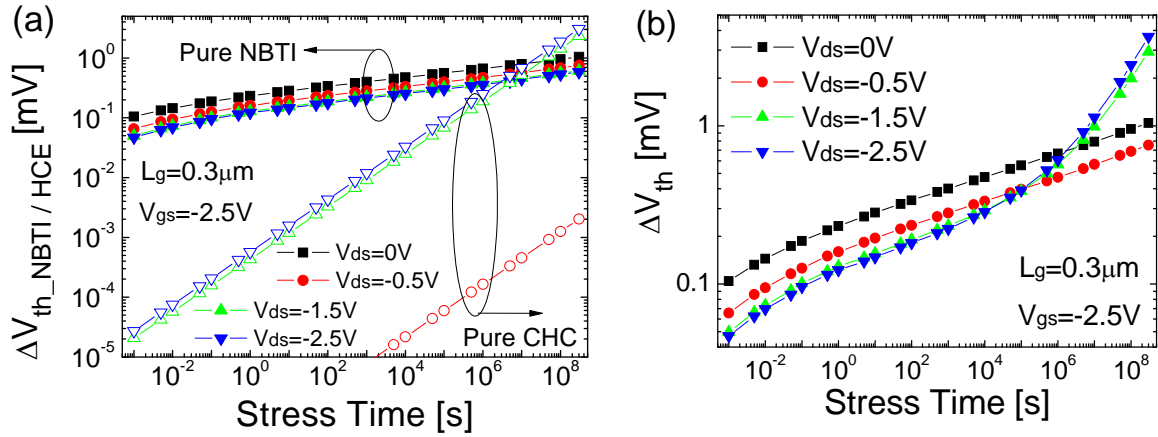


Fig. 4.4.7. Simulation results of (a) Separated and (b) cooperated contribution of NBTI and CHC to ΔV_{th} over wide stress time duration.

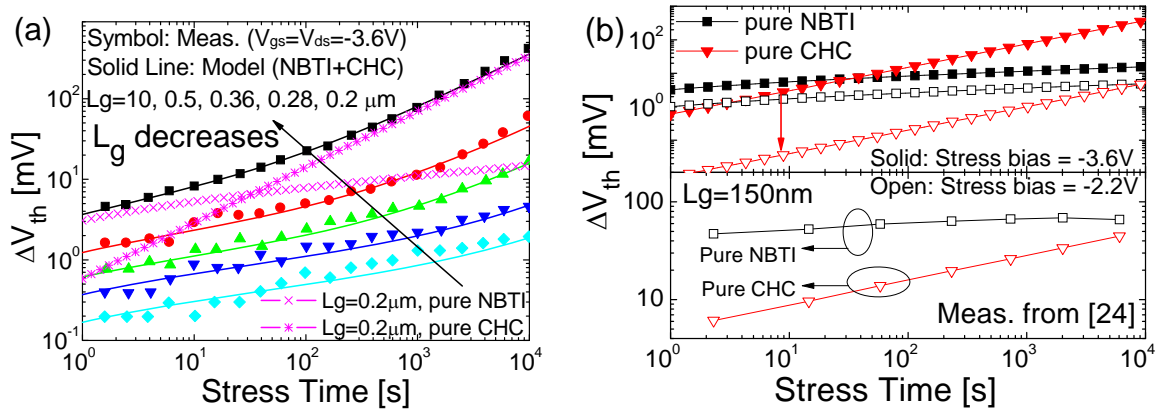


Fig. 4.4.8. The contributions of pure NBTI, pure CHC, and coupling effects to ΔV_{th} with gate length $L_g = 0.2 \sim 10 \mu m$ with stress $V_{gs} = V_{ds} = -3.6V$. (b) Simulation of the pure NBTI and CHC shift from $V_{gs} = V_{ds} = -3.6V$ to $-2.2V$ (upper figure). The simulation results are consistent with the measurement data [4.28] under $-2.2V$ stress with $L_g = 0.2 \mu m$ (lower figure).

Fig. 4.4.8(a) compares model results to measured data under stress condition of $V_{gs} = V_{ds} = -3.6V$ and channel length ranging from $0.2 \mu m$ to $10 \mu m$ [4.34]. As expecting from the

above investigation, the CHC effect dominates the long term degradation. With decreased channel length, the CHC effect is evidently enhanced and results in larger ΔV_{th} due to the increased I_{ds} and E_{max} , as demonstrated in Fig. 4.4.6. On the other hand, as shown in Fig. 4.4.8(b), when the stress bias is reduced to -2.2V, the CHC degradation shows larger reduction compared to the NBTI degradation. The simulation result [upper Fig. 4.4.8(b)] is consistent with the measurement [4.35] [lower Fig. 4.4.8(b)].

The recovery processes of the NBTI effect and CHC effect are modeled and compared with measurements [4.35] in Fig. 4.4.9. The stress bias is -2.2V, and the stress time ranges from 2.3s to 6000s. Compared with the NBTI degradation (in solid symbol) the CHC stress ($V_{gs}=V_{ds}=-2.2V$, in open symbol) results in less degradation at the initial stage and trends smaller recovery. Both the NBTI and the CHC recovery mechanisms show similar logarithmic time dependence, indicating that the recoverable ΔV_{th} is mainly due to the NBTI effect and is weakened by applying non-zero V_{ds} .

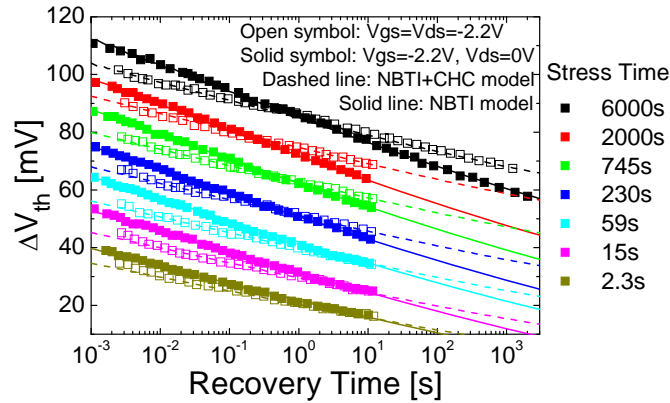


Fig. 4.4.9. ΔV_{th} recovery of NBTI ($V_{gs}=-2.2V$, $V_{ds}=0V$) and CHC ($V_{gs}=V_{ds}=-2.2V$) effects with stress times from 2.3s to 6000s. The model results agree well with the measured data [4.35].

4.5 Summary

This work developed a compact NBTI model including two independent mechanisms of the hole-trapping and the interface-state generation. By analyzing the measurement data under various bias conditions, the interface-state generation is observed dominating the degradation under high stress bias, especially in the long term region. Whereas the hole-trapping

dominates the degradation under high stress bias, as well as in the short term region. The developed model is also verified in the view of temperature dependence, and capable to reproduce the measurement results during both stress and recovery procedures, as well as the transition procedure between various temperature conditions. Considering the operation condition of the real circuit, the NBTI model is improved by containing the hot carrier effect induced by the applied V_{ds} . With increased V_{ds} , the NBTI effect is weakened due to the reduced vertical electric field in the gate oxide. At the same time, the CHC effect is enhanced by the increased lateral channel field. The model proves the accurate prediction of the “turn-around” mechanism of the threshold voltage shift as well as the stress/recovery time dependence of the ΔV_{th} under various gate lengths and bias conditions.

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Chapter 5 SPICE Level Simulation with the NBTI Model

5.1 Introduction

The final purpose of the reliability model is to be used for predicting the degradation of real circuits under any operation conditions. In this chapter, the developed NBTI model is implemented into the commercial simulator HSPICE for circuit simulation. Influence of model parameters change and simulation procedure are investigated, and the degradation simulation of some basic circuits is carried out.

5.2 Influence of Model Parameter Change

5.2.1 NBTI model parameter change

As introduced in Chapter 4, the NBTI model is composed with three components: interface-state generation, hole-trapping at the interface and oxide traps. The contributions of hole-trapping and interface state generation to ΔV_{th} are separated under high (Fig. 5.2.1(a)) and low (Fig. 5.2.1(b)) stress biases. Hole-trapping in the existing interface states saturates rapidly in the initial stage, while oxide traps increases with stress time following a power-law relationship. The interface-state generation dominates the degradation under high stress bias (-2.3V), especially in the long term region. When the stress bias is reduced to -1.2V, the contribution of the interface state generation decreases much more serious than hole-trapping mechanism. Therefore, the hole-trapping component dominates the degradation not only in the short term region, but also exceeds the interface state generation mechanism in the long term region.

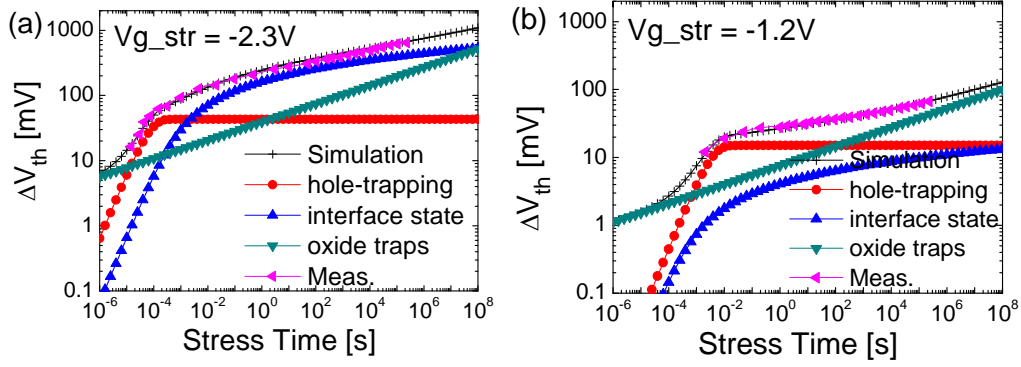


Fig. 5.2.1. The contributions of hole-trapping at the interface and in the gate oxide, as well as interface state generation to ΔV_{th} are separated under (a) High-voltage ($V_g = -2.3V$). (b) Low-voltage ($V_g = -1.2V$)

1) Interface-state generation rate R_{Eox}

$$\Delta V_{ths_int}(t) = \frac{q}{C_{ox}} \boxed{R_{Eox}} \log\left(1 + \frac{t}{\tau_s}\right)$$

- R_{Eox} is dependence on stress bias condition (see Chapter 4, Fig. 4.3.2(a)).
- NBTI induced ΔV_{th} decreases in parallel in the long term region.
- R_{Eox} doesn't impact ΔV_{th} in short term region.

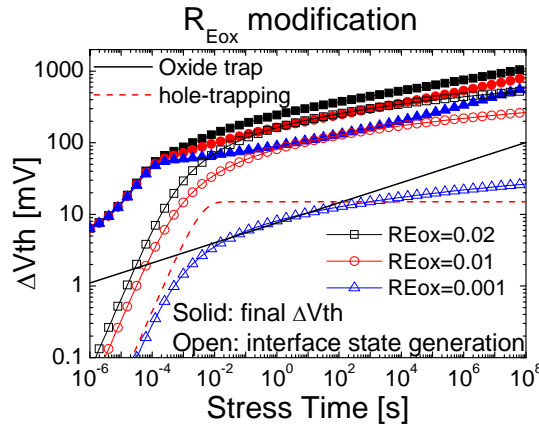


Fig. 5.2.2. Modification of the reaction rate R_{Eox} .

2) Interface state generation time constant τ_s

$$\Delta V_{ths_int}(t) = \frac{q}{C_{ox}} R_{Eox} \log\left(1 + \frac{t}{\boxed{\tau_s}}\right)$$

- τ_S is insensitive to the stress condition, but determined by processes.
- Interface state generation induced ΔV_{th} shift along time-axis in parallel
- τ_S impacts ΔV_{th} more obviously in the short term than in long term region.

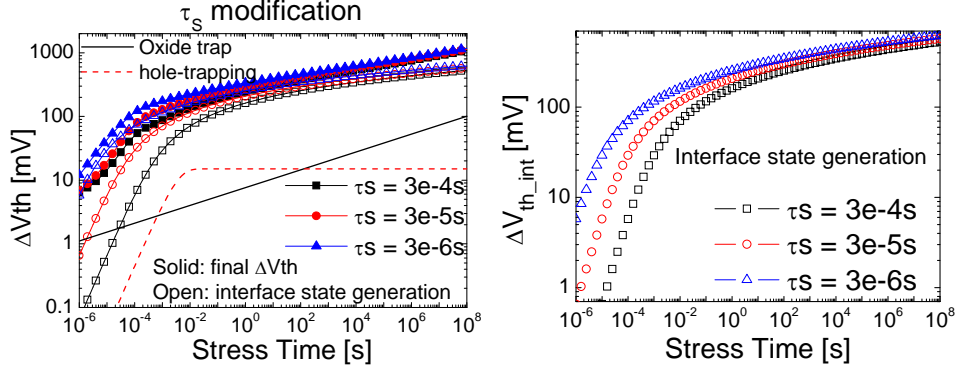


Fig. 5.2.3. Modification of the interface state generation time constant τ_S .

3) Existing hole-trap-site N_{int_trap}

$$V_{th_HT}(t) = \frac{q}{C_{ox}} N_{int_trap} \left[1 - \exp\left(-\frac{t}{\tau_c}\right) \right] = \boxed{V_{trap}} \left[1 - \exp\left(-\frac{t}{\tau_c}\right) \right]$$

- N_{int_trap} is dependence on stress condition (see Chapter 4, Fig. 4.3.2(b))
- Hole-trapping induced ΔV_{th} saturates fast and increases in parallel with increased N_{int_trap} .
- N_{int_trap} impacts the “turn-around” point, so that the increasing rate of ΔV_{th} .

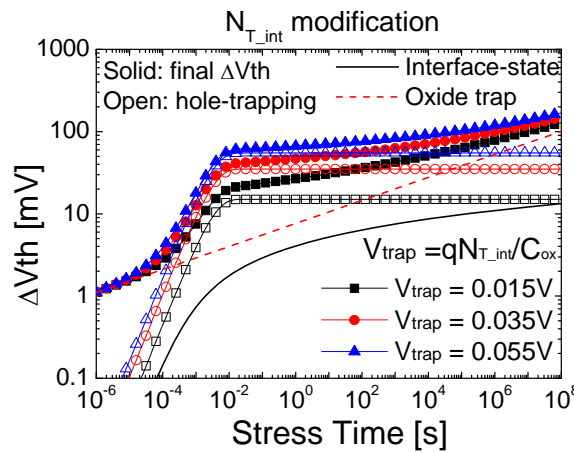


Fig. 5.2.4. Modification of the existing interface state generation time constant τ_S .

4) Hole-capture time constant τ_c

$$V_{th_HT}(t) = \frac{q}{C_{ox}} n_{T_int} \left[1 - \exp\left(-\frac{t}{\tau_c}\right) \right] = V_{trap} \left[1 - \exp\left(-\frac{t}{\tau_c}\right) \right]$$

- ❑ τ_c is dependence on the stress bias condition (see Chapter 4, Fig. 4.3.2(a))
- ❑ Hole-trapping induced ΔV_{th} shifts along time-axis in parallel.
- ❑ τ_c impacts ΔV_{th} in the short term region only.

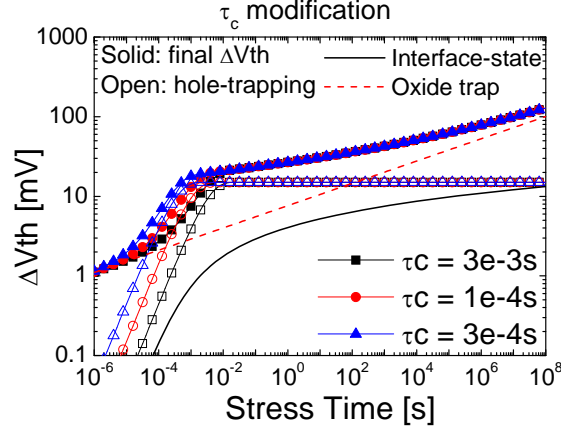


Fig. 5.2.5. Modification of the hole-capturing time constant τ_c .

5) Hole-injection density N_0

$$V_{th_ox} \approx \frac{q}{C_{ox}} \frac{N_0}{\lambda} (t / \tau_0)^n = V_{ox} (t / \tau_0)^n$$

- ❑ N_0 is dependence on stress condition (see Chapter 4, Fig. 4.3.2(b))
- ❑ Oxide traps induced ΔV_{th} shows a parallel shift with N_0 in log-log scale.
- ❑ N_0 impacts ΔV_{th} in both short term and long term regions

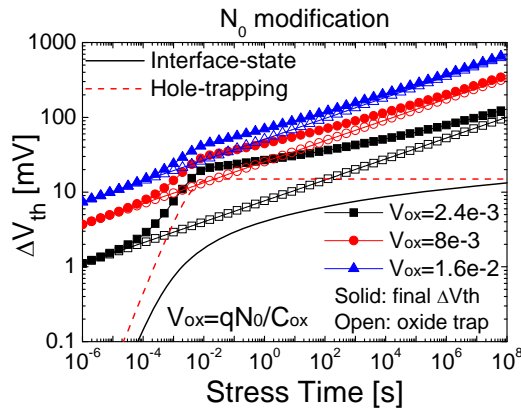
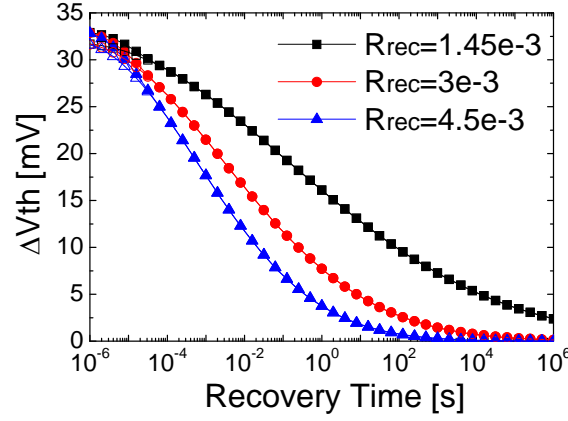


Fig. 5.2.6. Modification of the injected hole density N_0 .

6) Recovery rate R_{rec}

$$\Delta V_{th_int}^R(t) = \Delta V_{th_int}^{\max} - \Delta V_{th_int}^{\max} \cdot R_{rec} \log \left(1 + \frac{t}{\tau_{rec}} \right)$$

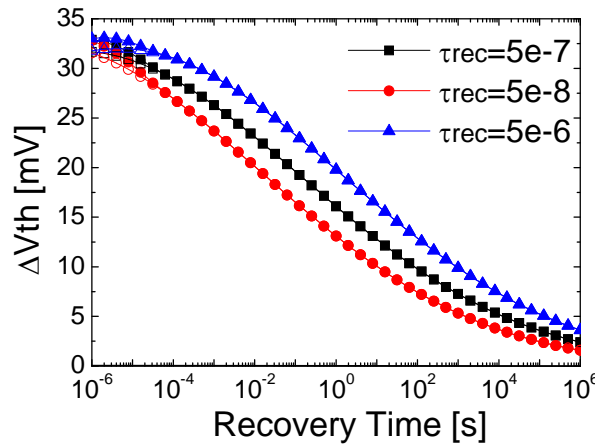
- R_{rec} is dependence to the stress time (see Chapter 4, Fig. 4.3.5)
- ΔV_{th} recovers faster with larger R_{rec}


 Fig. 5.2.7. Modification of the recovery rate R_{rec} .

7) Recovery time constant τ_{rec}

$$\Delta V_{th_int}^R(t) = \Delta V_{th_int}^{\max} - \Delta V_{th_int}^{\max} \cdot R_{rec} \log \left(1 + \frac{t}{\tau_{rec}} \right)$$

- τ_{rec} is insensitive to the stress time
- The un-recoverable ΔV_{th} component becomes larger with increased τ_{rec}


 Fig. 5.2.8. Modification of the recovery time constant τ_{rec} .

8) Emission time constant τ_e

$$\Delta V_{th_trap}^R = \Delta V_{th_trap}^{\max} \exp(-t / \tau_e)$$

- τ_e is insensitive to the stress time
- The hole-trapping recovery starts later with increased τ_e

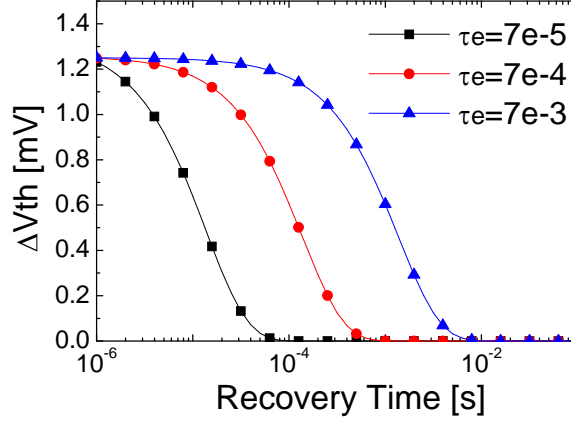


Fig. 5.2.9. Modification of the hole-emission time constant τ_e .

5.2.2 HCE model parameter change

1) Hot hole mean-free-path λ_{chc}

$$\Delta V_{th_CHC} = C \left\{ \exp[-\varphi_{it} / (q\lambda_{chc} E_{\max})] \cdot (I_{ds} / W) \cdot t \right\}^m$$

- CHC degradation tends to saturate with large λ_{chc} .

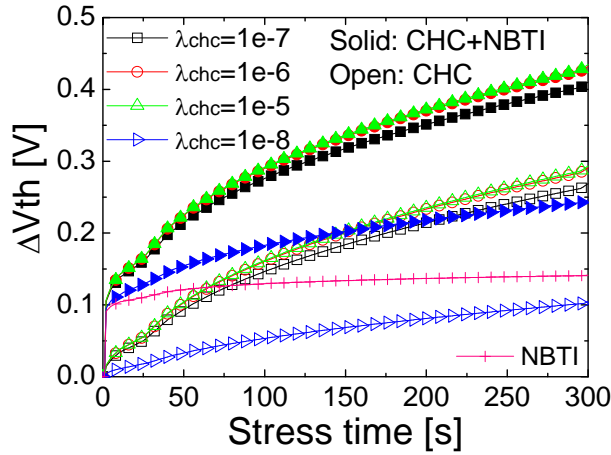
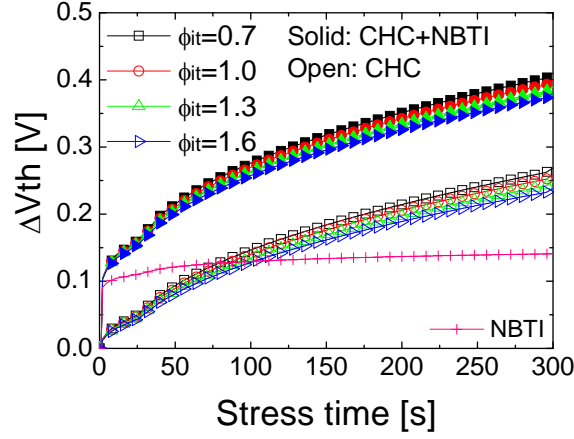


Fig. 5.2.10. Modification of the mean-free path of the hot hole λ_{chc} .

2) Critical energy for trap creating φ_{it}

$$\Delta V_{th_CHC} = C \left\{ \exp[-\varphi_{it} / (q\lambda_{chc} E_{\max})] \cdot (I_{ds} / W) \cdot t \right\}^m$$

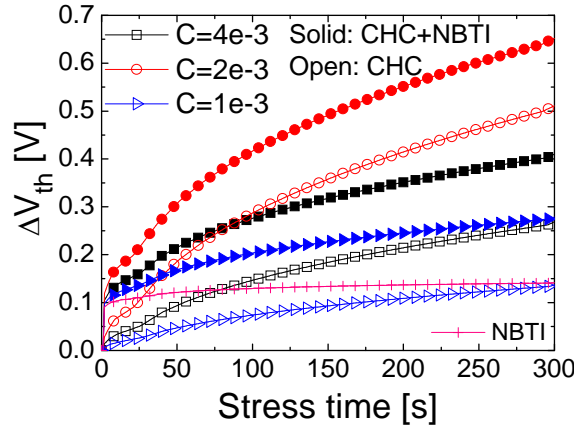
- CHC degradation becomes more slowly with increased φ_{it} .


 Fig. 5.2.11. Modification of the trap creation critical energy ϕ_{it} .

3) Fitting parameter C

$$\Delta V_{th_CHC} = C \left\{ \exp[-\phi_{it} / (q\lambda_{chc} E_{max})] \cdot (I_{ds} / W) \cdot t \right\}^m$$

■ The amplitude of CHC degradation increases with increased C .


 Fig. 5.2.12. Modification of the fitting parameter C .

5.3 SPICE level simulation

The predictive model including NBTI effect and CHC effect is implemented into HiSIM, and the flow chart is shown in Fig. 5.3.1. In the NBTI model, the flat band voltage ($V_{fb,i}$) and the vertical gate oxide field ($E_{ox,i}$) at the i^{th} time step (t_i) are first calculated with HiSIM ($E_{ox,i} = (V_g - V_{fb,i} - \phi_{s,i}) / T_{ox}$). Then NBTI induced ΔV_{th} [$\Delta V_{th_NBTI}(t_i)$] is obtained from Eq. (14).

Afterwards $\Delta V_{th_NBTI}(t_i)$ is added to $V_{fb,i}$ for the next-step calculation. In the CHC model, pinch-off-region length (ΔL), surface potentials at the source (ϕ_{s0}), drain junction [$\phi_s(\Delta L)$] and the pinch-off point (ϕ_{sL}) are obtained from HiSIM and used for calculating the maximum channel field E_{max} . With the calculated I_{ds} , the CHC induced ΔV_{th} [$\Delta V_{th_CHC}(t_i)$] is calculated.

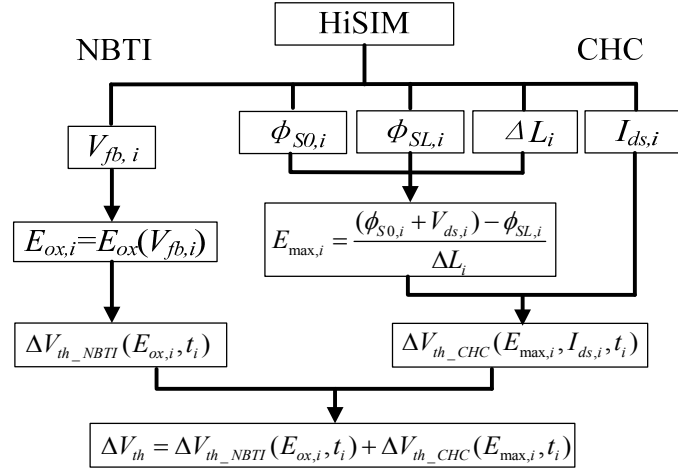


Fig. 5.3.1. Flow chart for implementation of NBTI and CHC models into HiSIM model.

The HiSIM model containing NBTI and HCE effects is written in Verilog-A and simulated with HSPICE. The simulation details including partial code and results are shown as follows:

1) Generate stress/recovery time of the NBTI effect

- The stress/recovery time for NBTI simulation starts from 0s.
- Stress/recovery time is generated by subtracting the previous stress/recovery time from the absolute transient time.

***** CODE BEGIN *****

```

if (Ig > 0) begin           // stress
    ts= $abstime ;         // last stress time point
end else begin              // recovery
    tr= $abstime;          // last recovery time point
end
    
```

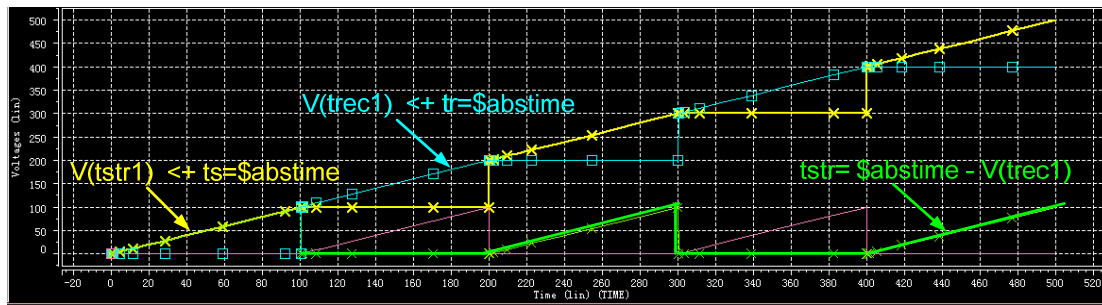
```
V(tstr1) <+ ts;
V(trec1) <+ tr;

tstr= $abstime - V(trec1); // stress time in each cycle
trec= $abstime - V(tstr1); // recovery time in each cycle
```

end

***** CODE END *****

Result



2) Stress time generation of the hot carrier effect

- CHC effect is assumed generating unrecoverable degradation.
- The stress time is accumulated only in the stress period, and keeps constant in the recovery period.

***** CODE BEGIN *****

if (Ig > 0) begin

```
t0 = 1; // used for time calculation
```

```
dVths_chc = f ( tcont ); // CHC degradation is function of stress time (tcont)
```

end else begin

```
t0 = 0; // used for time calculation
```

```
dVthr_chc = V(chcmax);
```

end

```
V(tnor) <+ t0; // normalized time to 1 (stress) and 0 (recovery)
```

```
V(tcontt) <+ (idt(V(tnor), 0)); // integrate the normalized time
```

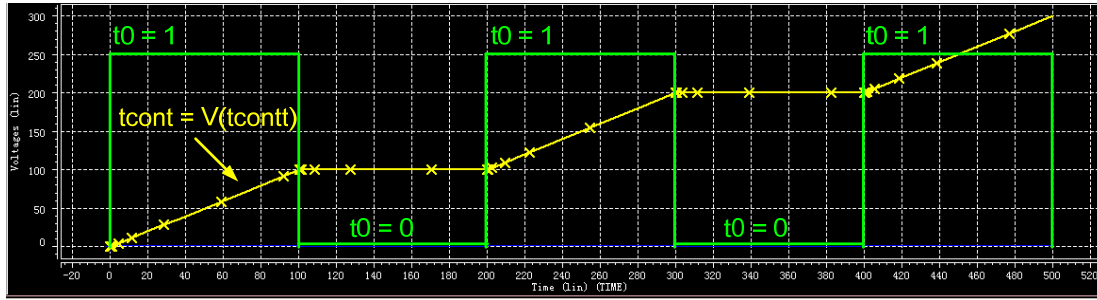
```
tcont = V(tcontt); // generate the monotonously increased time signal
```

```
V(chcmax) <+ dVth_chcs; // output maximum ΔVth induced by CHC effect
```

end

```
***** CODE END *****
```

Result



3) Varilog-A coding of hole-trapping

Notice: hole trapping/de-trapping from the existing trap-sites usually occurs very fast (with in 1s), the degradation is unable to be seen if the trap/de-trap time constant (τ_{trap} / $\tau_{\text{de-trap}}$) is too small. Therefore, in order to have a clear view of such mechanism, the time constant is enlarged for simulation.

Model

$$\Delta V_{\text{th_HT}}^{\text{S}} = \frac{qN_{\text{int_trap}}}{C_{\text{ox}}} [1 - \exp(-t / \tau_c)]$$

$$\Delta V_{\text{th_trap}}^{\text{R}} = \Delta V_{\text{th_trap}}^{\text{max}} \exp(-t / \tau_c)$$

```
***** CODE BEGIN *****
```

```
analog begin
```

```
if (Ig > 0) begin // stress
```

```
    Ntrap = A_trap * exp( B_trap * ( abs( V(gates)) - V(Vfbmin) ) );
```

```
                                // Trap density
```

```
    taus_trap = A_tautrap * exp( B_tautrap * ( abs( V(gates)) - V(Vfbmin) ) );
```

```
                                // Trap time constant
```

```

dVths_trap = V(trapmin) + (Ntrap - V(trapmin)) * (1-1*exp(- tstr / taus_trap));
// ΔVth induced by hole-trapping

end else begin // recovery

dVthr_trap = V(trapmax) * exp(-trec / taur_trap); // ΔVth induced by hole-detrapping

end

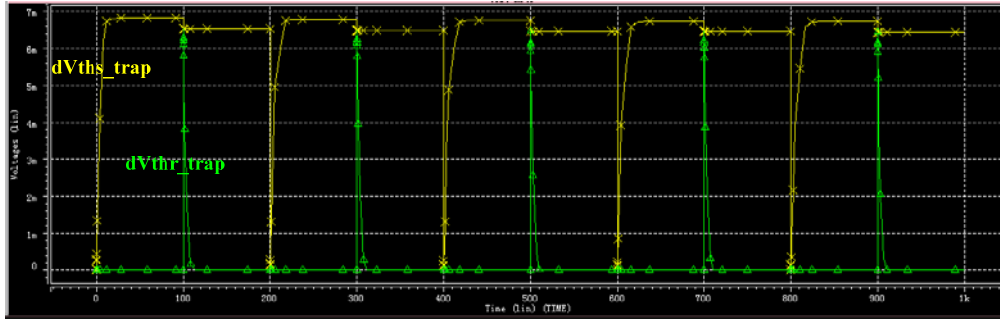
V(trapmax) <+ dVths_trap; // Maximum ΔVth after stress
V(trapmin) <+ dVthr_trap; // Minimum ΔVth after recovery

end

***** CODE END *****

```

Result



4) Varilog-A coding of interface state generation

Notice: The reaction rate (R_{Eox}) is function of stress bias.

Model

$$\Delta V_{\text{th_int}}^{\text{S}}(t) = \frac{q}{C_{\text{ox}}} \cdot R_{\text{Eox}} \cdot \log\left(1 + \frac{t}{\tau_{\text{S}}}\right)$$

$$\Delta V_{\text{th_int}}^{\text{R}}(t) = \Delta V_{\text{th_int}}^{\text{max}} - \Delta V_{\text{th_int}}^{\text{max}} \cdot R_{\text{rec}} \log\left(1 + \frac{t}{\tau_{\text{rec}}}\right)$$

```

***** CODE BEGIN *****

```

analog begin

```

if (Ig > 0) begin // stress

    REox = A_Reox * exp (B_Reox * (abs(V(gates)) - V(Vfbmin) ) );

```

```

// interface generation rate,  $E_{ox}$  dependent
dVths_int = V(intmin) + REox * log(1+ tstr / taus);

// interface state generation

end else begin // recovery
    dVthr_int = V(intmax) - V(intmax) * Rrec * log( 1+ trec / taur);

// interface state annealing

end

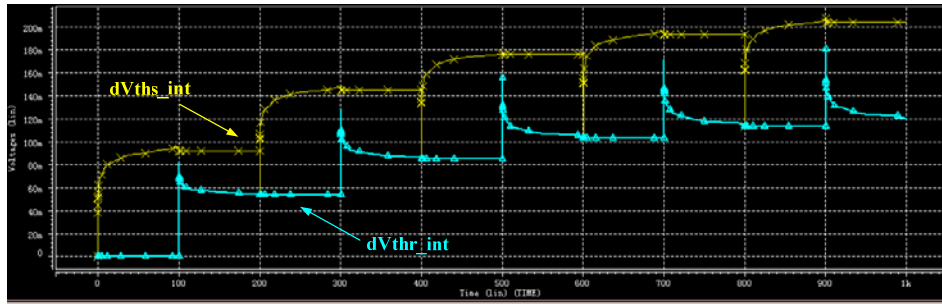
V(intmax) <+ dVths_int; // Maximum  $\Delta V_{th}$  after stress
V(intmin) <+ dVthr_int; // Minimum  $\Delta V_{th}$  after recovery

end

***** CODE END *****

```

Result



5) Varilog-A coding of oxide trap generation

Notice: The oxide traps are supposed generated without recovery even after the stress bias is removed. The stress time is the same as CHC. The injected hole density (N_0) is relative to the gate leakage, which follows an exponential function of gate bias ($N_0 \sim \exp(-1/V_{gs})$).

Model

$$n_{T_{ox}} \approx \frac{N_0}{\lambda} \left(t / \tau_0 \right)^n = \frac{N_0}{\lambda} \left(D_{polyf} t \right)^n$$

```
***** CODE BEGIN *****
```

analog begin

```

if (Ig > 0) begin // Stress
    delta_Vgs = abs(V(gates)) - V(Vfbmin);

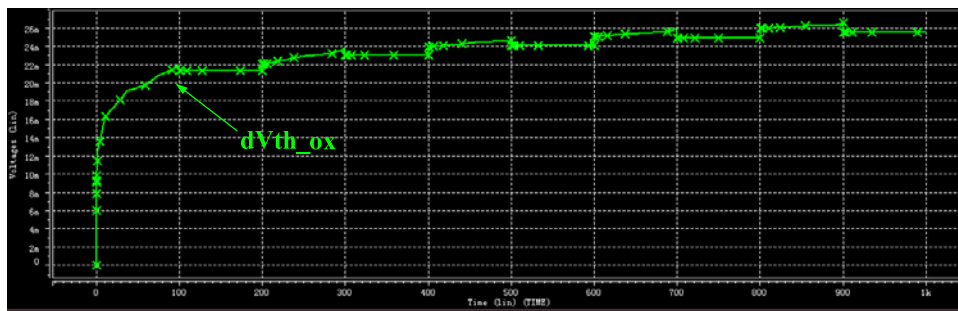
```

```

// Gate bias applied subtracting the Vfb degradation
Nox = A_NoX * exp(-(B_NoX / (delta_Vgs + 1e-20))); // Injected hole density
dVths_ox = Nox * ( pow ( ( Dpolyf * tcont ), sita ) ); // oxide traps
end else begin // Recovery
dVths_ox = V(oxmax) ; // Maximum  $\Delta V_{th}$  induced by oxide traps
end
end
***** CODE END *****

```

Result



6) Varilog-A coding of CHC effect

Model

$$\Delta V_{th_CHC} = C \left\{ \exp[-\varphi_{it} / (q\lambda_{chc} E_{max})] \cdot (I_{ds} / W) \cdot t \right\}^m$$

```
***** CODE BEGIN *****
```

```
analog begin
```

```
if (Ig > 0) begin // stress
```

```
Emax_xqy1 = (Pdrain - Psdl)/XQY; // Maximum channel field
```

```
dVth_chcs = m_chc * pow((exp(-Pit/lamda/Emax_xqy1)* tcont* abs(IdS)/W),0.5);
```

// ΔV_{th} induced by CHC

```
end else begin // recovery
```

```

dVth_chcr = V(chcmax) ; // Hold maximum  $\Delta V_{th}$  during the recovery process
end

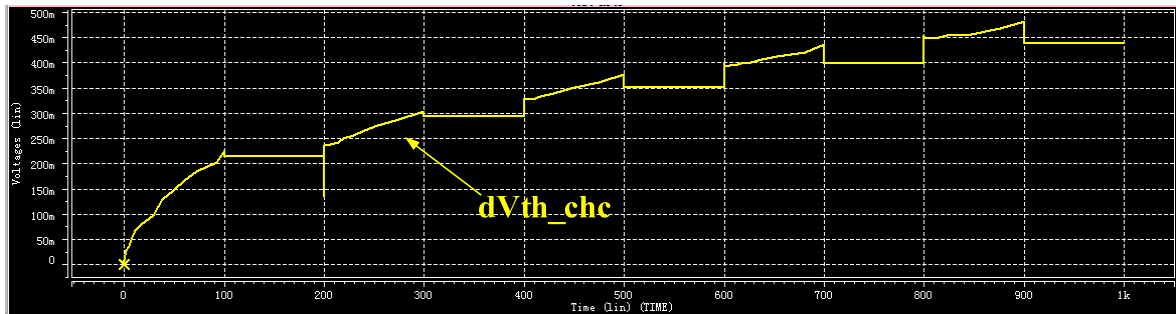
V(chcmax) <+ dVth_chcs;

end

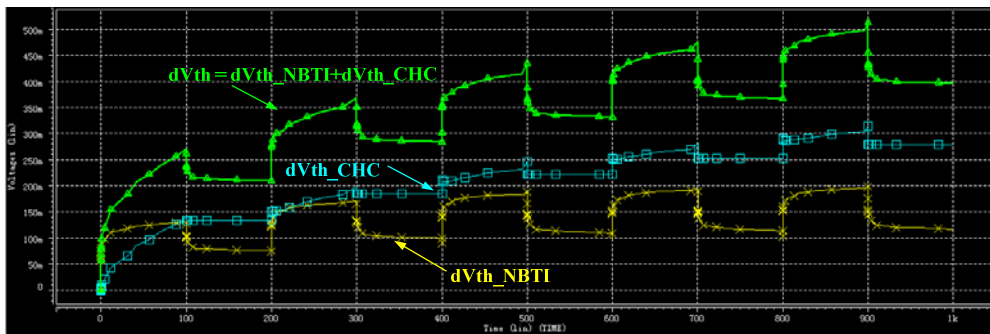
***** CODE END *****

```

Result



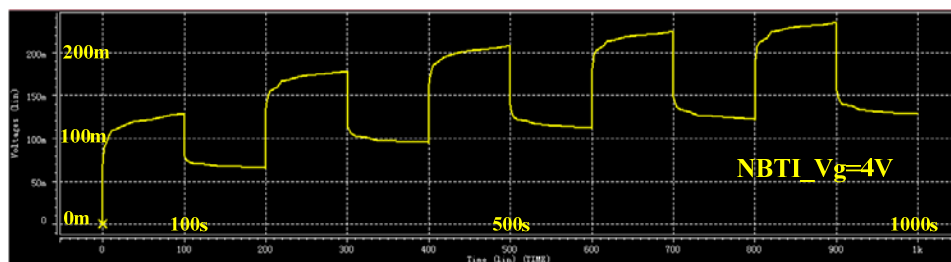
7) ΔV_{th} including NBTI effect and CHC effect



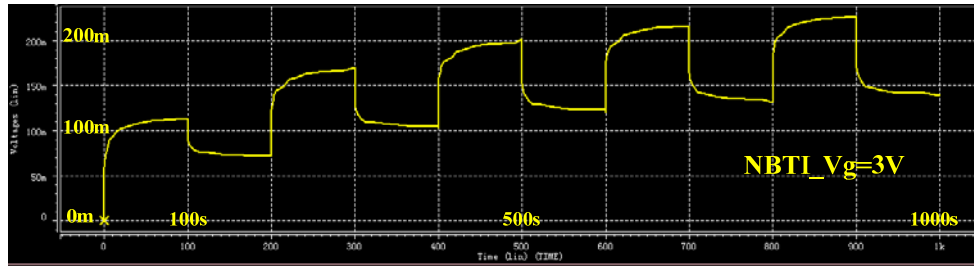
8) V_g dependence of NBTI effect

ΔV_{th} induced by NBTI effect decreases with decreased V_{gs} .

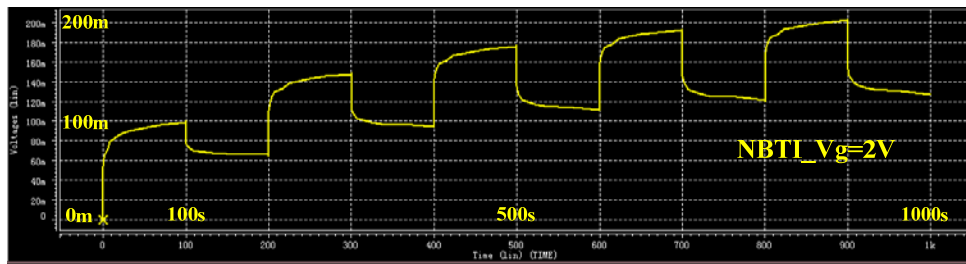
$V_g = -4V$



$V_g = -3V$



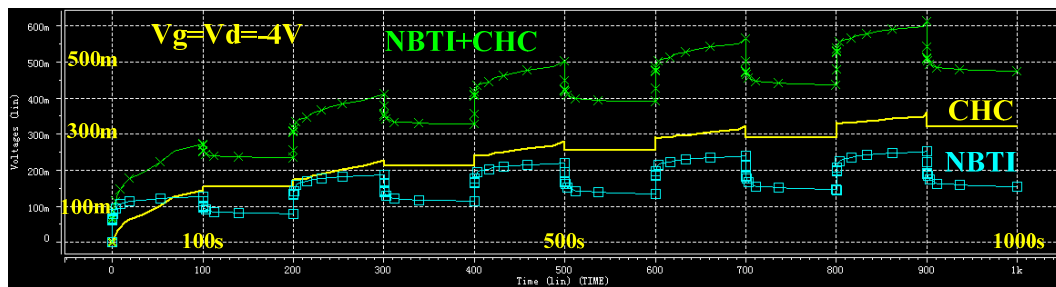
$V_g = -2V$



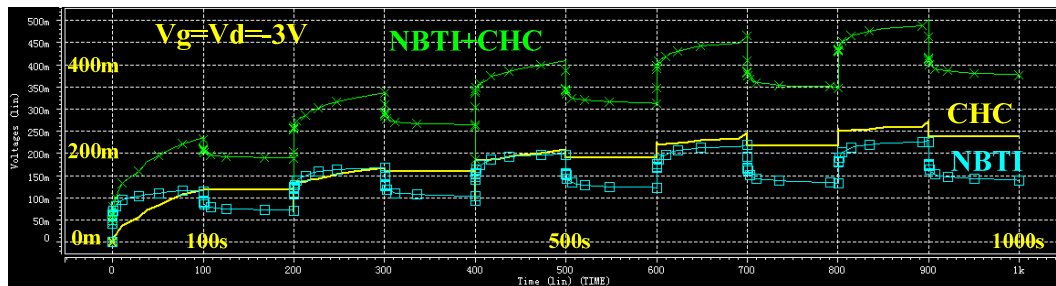
9) V_{ds} dependence of CHC effect

ΔV_{th} induced by CHC effect decreases with decreased V_{ds} , and even lower than that induced by NBTI effect.

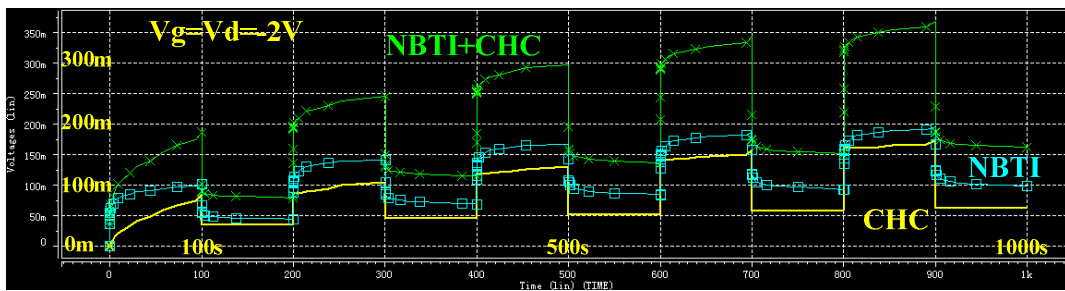
$V_g = V_d = -4V$



$V_g = V_d = -3V$



$V_g=V_d=-2V$

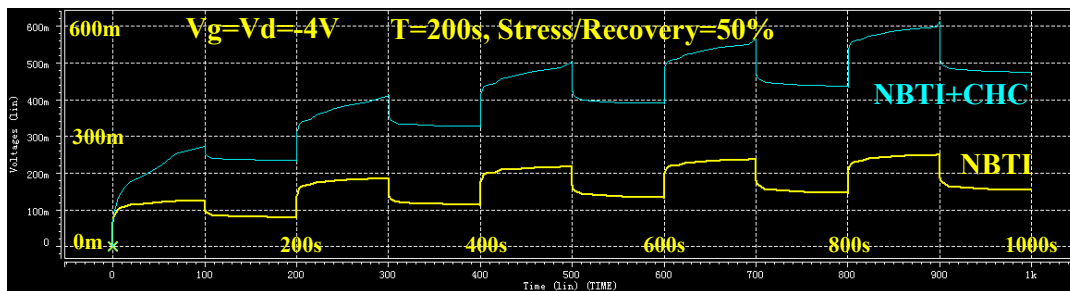


10) Frequency dependence of CHC effect

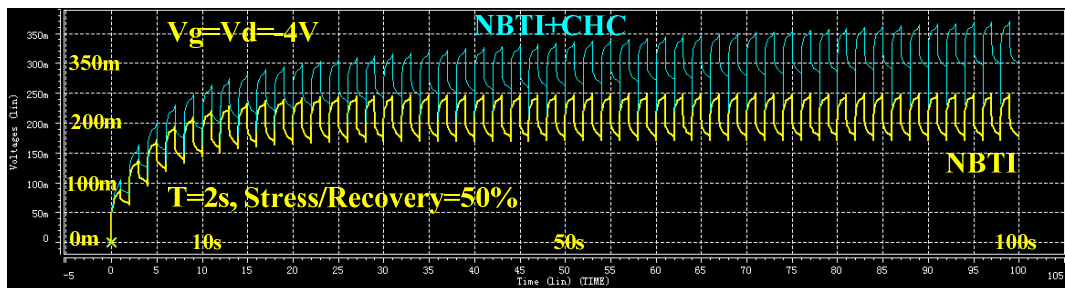
Both NBTI and CHC degradations decrease with increased frequency. Compared to NBTI component, the proportion of CHC component reduces under high frequency.

$V_g=V_d=-4V$, Stress/Recovery = 50%

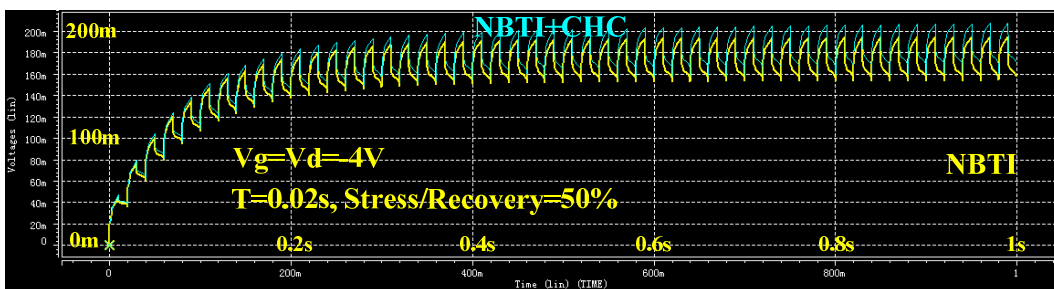
$T=200s$



$T=2s$



$T=0.02s$



11) Circuit simulation

Degradation induced by NBTI effect and CHC effect results in the output delay of both inverter and NAND. Fig. 5.3.2 (a) and (b) shows frequency dependence and duty cycle dependence of the delay time (t_{delay}) of a resistive-load inverter with the supply voltage $V_{\text{dd}}=1.2\text{V}$ and the resistance $R=2e5\Omega$. Considering that the circuit delay is mainly due to the unrecoverable degradation of the p-MOSFET, therefore, the delay time is determined by the minimum ΔV_{th} , which increases with the increased frequency, as shown in Fig. 4.3.8 of Chapter 4. Observed from Fig. 5.3.2 (a), the delay time degradation tends to saturation with high frequency. Such phenomenon is supposed due to the limitation of the hole-capture/emission time of the existing traps. No carrier exchange between traps and substrate occurs under ultra high frequency. As shown in Fig. 5.3.2 (b), the duty cycle dependence of t_{delay} is investigated. Here the 100% duty cycle indicates DC stress without recovery, and causes worst degradation. With decreased duty cycle, the delay time reduces due to shorter stress time but longer recovery time during each duty.

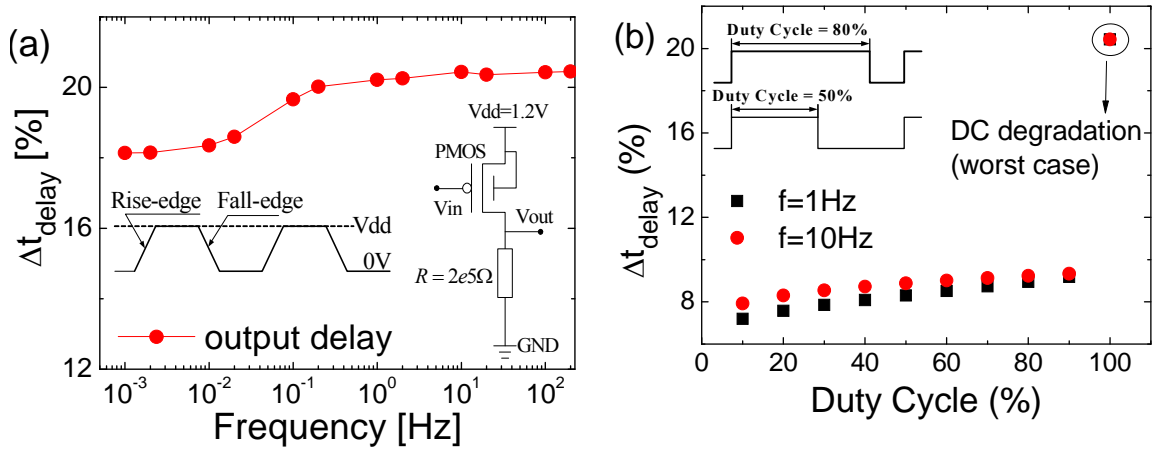


Fig. 5.3.2. (a) Frequency dependence and (b) Duty cycle dependence of the output delay (t_{delay}) in a resistive-load inverter.

Similar simulation is carried out in NAND, as shown in Fig. 5.3.3. The input signal of device B (inB) is fixed at high bias V_{dd} , and the input signal of device A (inA) is with various frequency and duty cycle. The results are similar to the observation of inverter. The frequency dependence of both inverter and NAND are simulated consistent with the measured data from various research groups [5.1]

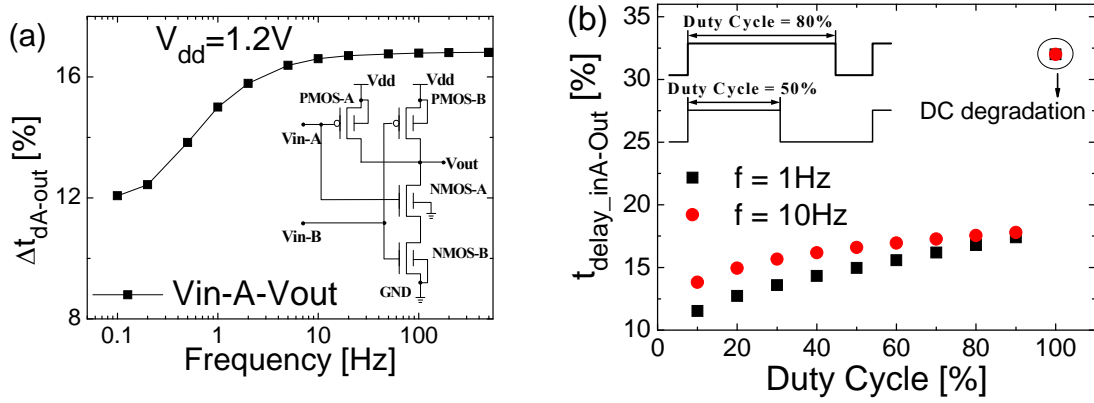


Fig. 5.3.3. (a) Frequency and (b) duty cycle dependence of NAND delay degradation.

Fig. 5.3.4 simulates the degradation of 21-stage oscillator during 10 years' operation. The output delays of the 4th, 10th and 20th stages are taken for instance. Higher stage exhibits larger delay due to the accumulation effect of the previous inverters. The delay time degradation approximately features power-law time dependence, which is consistent with the results reported [5.2].

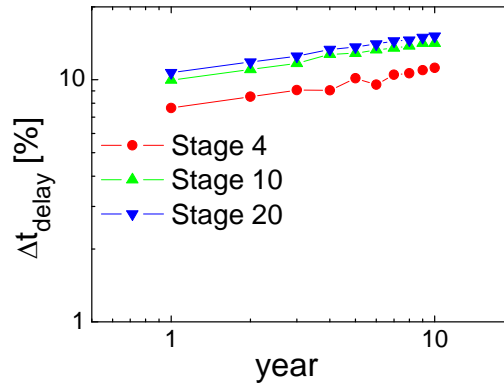


Fig. 5.3.4. Delay time degradation of the stages 4, 10 and 20 during 10 years' operation.

5.4 Summary

In this chapter, the influence of model parameters to the simulation result is investigated by modifying the parameters. The simulation procedures in SPICE level are discussed in detail, and the degradation caused from NBTI effect and hot carrier effect has been separated under various conditions. The frequency dependence and duty cycle dependence of the resistance-load inverter, NAND and 21-stage oscillator are simulated using HSPICE, and the

performance degradation during circuit operation are predicted using HiSIM model coupled with NBTI model.

References

- [5.1] S. Mahapatra, A. E. Islam, S. Deora, V. D. Maheta, K. Joshi, A. Jain and M. A. Alam, “A Critical Re-evaluation of the Usefulness of R-D Framework in Predicting NBTI Stress and Recovery,” *IEEE International Reliability Physics. Symposium. (IRPS 2013)*, pp. 614-623, 2013.
- [5.2] Pong-Fei Lu and Keith A. Jenkins, “A built-in BTI monitor for long-term data collection in IBM microprocessors,” *IEEE International Reliability Physics. Symposium. (IRPS 2013)*, pp. 4A.1.1-4A.1.6, 2013.

Chapter 6 Conclusions

In this thesis, a predictive compact model for the NBTI effect has been developed. Since hydrogen reaction-diffusion and hole-trapping mechanisms are accepted as two possible origins the NBTI degradation, the model is developed based on these two theories. Considering that an efficient NBTI model has to be able to accurately predict the following features: 1) long term degradation under DC stress conditions, 2) AC degradation with various frequencies and duty cycle, 3) the recovery characteristic in short term and long term regions and 4) temperature dependence, new physical insight and modeling are introduced in the developed compact NBTI model. The main achievements of this thesis are shown in the following:

- 1) In the developed reaction-limited-diffusion NBTI model, the reaction process of Si-H bond is described by using a dynamic balance equation. The forward reaction rate is supposed decreasing with increased stress time due to the accumulation of H atoms within the gate oxide. The diffusion mechanism of H atoms including the diffusion within the gate oxide and enter into the poly-Si gate, which the H atoms are transferred into H₂ molecules. Combining with the hole-trapping mechanism, the NBTI model based on the hydrogen reaction-diffusion theory is developed and shows a good agreement with the measured data under both DC and AC conditions.
- 2) As investigated using ultra fast measurement technologies, the hydrogen-diffusion theory began to show its limitation in describing the degradation during the recovery and high frequency NBTI effect. Hole-trapping theory has been widely accepted explanation for logarithmic time dependence of V_{th} degradation. The reaction-limited-diffusion model developed in the previous chapter is further developed by considering the interface state generation mechanism due to the silicon bond dissociation. The influence of the generated interface state is added into the calculation of the gate oxide field, therefore, the logarithmic time dependence of ΔV_{th} is physically derived. Combining with the hole-trapping

theory, the newly developed NBTI model becomes more reasonable and effective in describing the degradation under various conditions, including stress bias, stress/recovery processes, technologies and materials, frequency dependence and duty cycles.

- 3) Considering the operation condition of p-MOSFET in real circuit, the influence of the applied drain bias to the degradation is unable to be neglected due to the evidently enhanced channel lateral electrical field. In this thesis we developed the hot carrier effect model using the classical expression and calculated the key parameters with the compact model HiSIM. Combining both NBTI and hot carrier effect model, the threshold voltage degradation under any operation conditions are able to be predicted.
- 4) In order to carry out the prediction of circuit performance, the developed NBTI model is implemented into compact device model HiSIM. The degradation of the threshold voltage is equivalent to the shift of flat-band voltage, which directly impacts the electric field, potential and current. Therefore the performance degradation of the circuit is able to be simulated.

Acknowledgment

Besides of being a summary of my three-year's study, this thesis gathers a lot of love from many professors, classmates, friends and family members. Here I want to express my sincere appreciation to all of them.

First of all, I have to give my highest appreciation to my supervisor, Prof. Mitiko Miura-Mattausch. Without her help and encouragement, it is impossible for me to have a smooth research experience and happy life in Japan. Her deep understanding of device physics leads me to approach my reliability study from the physics level, but not focus only on the observation of experimental phenomenon. With her support, I am able to get numerous opportunities to communicate with other researchers around the world. I can not imagine how life will be without her kindness. Hopefully I didn't disappoint her so much during the past three years.

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