

**Crystallization of Amorphous Silicon Films  
by Atmospheric Pressure Micro-Thermal-Plasma-Jet Irradiation  
and Its Application to Thin-Film Transistors**

大気圧マイクロ熱プラズマジェット照射によるアモルファスシリコン膜の  
結晶化及び薄膜トランジスタへの応用

Shohei Hayashi

Graduate School of Advanced Sciences of Matter, Hiroshima University

**Abstract**

Thin-film transistor (TFT) is the most important key device in flat panel displays (FPDs). With the remarkable spread of mobile devices such as a smart-phone and tablet personal-computer, FPDs need higher performance and lower electricity consumption. For back-planes of liquid crystal display (LCD), a hydrogenated-amorphous Si (a-Si:H) TFT has been widely utilized because one can be fabricated uniformly in large area substrates. However, lower mobility and reliability of a-Si:H TFT are serious problems for fabrication of higher resolution FPDs and application to an organic light emitting diode (OLED) displays. A crystalline-Si (c-Si) TFT is very promising as the next generation TFTs because of their high mobility, high reliability, and ability to fabricate complementary metal-oxide-semiconductor (CMOS) circuits.

In the fabrication of c-Si TFTs, the crystallization of a-Si films is one of the most important processes. I have proposed in this thesis a new technique to crystallize a-Si films using a micro-thermal-plasma-jet ( $\mu$ -TPJ) for fabrication of high-performance TFTs. In addition, I investigated the mechanism of grain growth by using a new *in-situ* observation technique.

In previous studies, TPJ was applied to crystallization of a-Si films. Amorphous-Si films were crystallized by TPJ irradiation in the solid phase (SPC), and the crystallized Si films were formed with small grains  $\sim 20$  nm in diameter. Although the TFTs fabricated by SPC-Si films had very high uniformity, the field-effect mobility ( $\mu_{FE}$ ) of these TFTs was  $\sim 10$  cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> [1]. To achieve higher  $\mu_{FE}$ , an enlargement of Si grains is required. Therefore, we attempted to melt a-Si films and to induce long lateral growth by using a TPJ with higher power density. To achieve the higher power density, we reduced the nozzle

diameter and increased the electrode spacing of a conventional TPJ. The reduced TPJ nozzle diameter increases the plasma density because it promotes a thermal pinch effect from the Cu anode cooled by water. The increased electrode spacing causes the plasma temperature to increase because it promotes joule heating as the resistance in thermal plasma increases [2]. As a result, the power density increased from 8.3 to 53.2 kWcm<sup>-2</sup>, which was higher than that of a continuous-wave (CW) laser (~30 kWcm<sup>-2</sup> [3]). We refer to this higher-power-density TPJ as “ $\mu$ -TPJ.” This result indicates that  $\mu$ -TPJ can anneal with high efficiency.

Amorphous-Si films were crystallized by  $\mu$ -TPJ irradiation. We directly observed the Si films during  $\mu$ -TPJ irradiation by using a high-speed camera. The reflectivity of Si changes significantly with phase transformations, which enabled clear observation of melting and regrowth. We investigated the crystallization mechanism by using an *in-situ* observation technique. First, an a-Si film was crystallized by SPC, and wave-like patterns were formed by a new crystallization mode called “leading wave crystallization (LWC).” An oval-shaped molten region was formed after inducing LWC, and the grains grew in a direction perpendicular to the liquid-solid interface. This lateral grain growth can be induced at a very high speed of 4000 mm/s; thus, we call this crystallization mode high-speed lateral crystallization (HSLC).

We attempted to investigate the LWC mechanism to further understand the grain growth. Observation at a higher time resolution indicated that grain growth that was much faster than the scanning speed was induced periodically in the LWC region. In addition, the wavelength increased with the increase in film thickness, which indicates that latent heat plays a very important role in driving the very high-speed growth. These growth phenomena strongly suggest that LWC is quite similar to explosive crystallization (EC) [4]. The driving force of conventional EC is the released latent heat at the liquid-amorphous interface, whereas EC propagates laterally into the SPC region in the LWC case. The model for one period of LWC was introduced, and numerical calculations were conducted in order to explain the experimental results quantitatively. It was clarified from the proposed model that the basic LWC mechanism is the formation of a thin liquid layer and the explosive movement driven by the released latent heat due to the phase transformation. These results indicate that the grain growth mechanism was successfully investigated by using a direct observation technique with the high-speed camera and by doing numerical calculations. This observation technique is difficult with CW laser crystallization because the transmitted laser destroys the high-speed camera. Therefore, it is necessary to contrive a different optical setting.

We attempted to characterize Si films crystallized by different growth modes. SPC-Si

films were composed of microcrystalline grains with a typical size of  $\sim 20$  nm, which results in a lower crystalline volume fraction of  $\sim 70\%$ . With LWC, wave-like periodic patterns were formed, and lateral growth was induced radially. The typical grain width was  $\sim 5$   $\mu\text{m}$ , and the length was several tens of micrometers. Dendritic grain growth was induced in the case of HSLC. The typical grain width and length were  $\sim 20$  and  $\sim 100$   $\mu\text{m}$ , respectively. Crystalline volume fractions of 100% were achieved in both LWC and HSLC because of the enlarged grain size. The electrical characteristics of these crystallized-Si films were investigated using TFTs that were fabricated by applying these crystallization modes to the channel regions. The SPC-Si TFT had lower ON current and  $\mu_{\text{FE}}$  of  $\sim 2$   $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  because the channel region contained many grain boundaries (GBs). The variations ( $1\sigma$ ) of the  $\mu_{\text{FE}}$  and threshold voltage ( $V_{\text{th}}$ ) were 1.69% and 1.44%, respectively. Channel regions formed by microcrystalline grains oriented randomly are isotropic in nature, which results in very high uniformity of TFT characteristics. In contrast, LWC- and HSLC-Si TFTs had very high  $\mu_{\text{FE}}$  larger than  $300$   $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  in the n-channel. The channels of these TFTs were formed by single grains. However, the  $V_{\text{th}}$  and sub-threshold swing ( $S$ ) value were markedly different between the LWC- and HSLC-Si TFTs. To investigate this difference, the characteristics of TFTs formed with light doping channels were measured, and defect densities were indirectly investigated. The results revealed that LWC-Si channels contained more defects than HSLC-Si channels. This suggests that LWC was induced by very high-speed grain growth, which results in the formation of many in-grain defects. Consequently, HSLC was found to be most effective to obtain high-performance TFTs.

Channel regions contain random GBs, which results in degradation of TFT characteristics. Therefore, it is necessary to control the grain growth in order to fabricate high-uniformity TFTs. We tried to control the grain growth direction by crystallizing narrow a-Si strips. Random GBs are known to be electrically active GBs and are formed by the collision of liquid-solid interfaces. By patterning a-Si films into narrow strips, the collision of liquid-solid interfaces can be suppressed. As a result, the number of random GBs was reduced with the decrease in strip width. This technique was applied to the TFT fabrication. TFT characteristics improved with the decrease in channel width because of the reduction in random GBs. The  $\mu_{\text{FE}}$  of  $520$   $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$  was the highest TFT performance ever achieved by a plasma crystallization technique. These results demonstrate that the  $\mu$ -TPJ crystallization technique is very effective for fabricating high-performance TFTs.

To achieve both high mobility and uniformity, a technique to control grain growth that includes GBs, crystal orientation, and in-grain defects is essential, although difficult to achieve. It is necessary to resolve this difficult issue in the future. Although random GBs

can be removed by crystallization of narrow a-Si strips, electrically inactive GBs such as  $\Sigma 3$  coincident site lattice and low angle GBs cannot be removed yet. The crystalline orientation changes with the formation of those GBs, which causes characteristic TFT variations because the carrier mobility depends on the crystalline orientation [5]. Therefore, controlling the GBs and orientation is very important in order to achieve high-uniformity TFTs. In addition, single-grain channel regions formed by HSLC have a few in-grain defects. To fabricate higher mobility TFTs, it is necessary to form channels with no defects.

## References

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